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INVESTIGATION OF SILICON CCD DELAY LINES. (U)
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U.S. GOVERNMENT PRINTING OFFICE: 1967
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RADC-TR-81-274
Final Technical Report
January 1982

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INVESTIGATION OF SILICON CCD DELAY LINES

Raytheon Company

**D. E. Greetham
J. P. Sage**

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER RADC-TR-81-274	2. GOVT ACCESSION NO. AD-A114	3. RECIPIENT'S CATALOG NUMBER 542
4. TITLE (and Subtitle) INVESTIGATION OF SILICON CCD DELAY LINES		5. TYPE OF REPORT & PERIOD COVERED Final Technical Report 29 Sep 78 - 31 Dec 80
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) D. E. Greetham J. P. Sage		8. CONTRACT OR GRANT NUMBER(s) F19628-78-C-0167
9. PERFORMING ORGANIZATION NAME AND ADDRESS Raytheon Company Missile Division Bedford MA 01730		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61101F 2305J130
11. CONTROLLING OFFICE NAME AND ADDRESS Deputy for Electronic Technology (RADC/ESE) Hanscom AFB MA 01731		12. REPORT DATE January 1982
		13. NUMBER OF PAGES 72
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Same		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report) Same		
18. SUPPLEMENTARY NOTES RADC Project Engineer: Paul W. Pellegrini (ESE)		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) High Speed Delay Lines Analog Delay Lines CCD I/O Circuits		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report describes the work performed under Contract No. F19628-78-C-0167 entitled "Investigation of Silicon CCD Delay Lines." The primary objectives of the contract include the analysis, design, and development of advanced CCDs with input and output circuitry as well as delay stages capable of operation at 100 MHz and above clock frequency. A high speed 256 stage CCD delay line with high frequency input and output circuits was designed. The device, circuit and process designs adopted emphasize		

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
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1. INTRODUCTION

This report describes the work performed under USAF contract No. F19628-78-C-0167 entitled "Investigation of Silicon CCD Delay Lines." The primary objectives of the contract include the analysis, design, and development of advanced CCDs with input and output circuitry as well as delay stages capable of operation at 100 MHz and above clock frequency.

A high speed 256 stage CCD delay line with high frequency input and output circuits was designed.

The device, circuit and process designs adopted emphasize future growth potential such that performance characteristics may be extended to much higher operating frequencies in the future.

2. THEORETICAL ANALYSIS OF CCD INPUT/OUTPUT STRUCTURES

2.1 Purpose and Basic Approach

Considerable effort has been devoted in the past to theoretical analysis of the transport of charge from gate to gate in the main channel of a CCD. Relatively little effort has been applied to a theoretical evaluation of charge flow limitations in the input and output structures in which conversions are made between external signals and charge in the CCD. Some of the results of the charge transfer efficiency studies can be carried over, but there are significant differences.

Since the effects of charge transfer loss accumulate over hundreds or even thousands of transfers, residual charges in the order of 10^{-3} , 10^{-4} , or 10^{-5} are of interest and concern. The I/O structures typically occur only once, and errors do not accumulate. Charge residues affect primarily only the linearity and secondarily, as will be seen later, the noise level of the conversions. Buried channel and short gate structures appropriate to very high speed CCDs have intrinsic nonlinearities of a few percent to begin with, and thus charge residues in the orders 10^{-1} and 10^{-2} are of interest in an analysis of I/O performance.

Another significant difference is that the transfer of charge from one gate to the next has a relatively simple formulation with boundary conditions that permit closed-form mathematical expressions to be found for special cases. The input/output structures and processes are more complex. Numerical analysis is therefore the primary tool for solving the equations, although the results of the numerical analyses may suggest simpler and useful ad hoc models.

The theoretical problem posed by the real CCD I/O structures is far too complex for practical solution even by numerical means. A high speed buried channel structure must be treated in at least two dimensions, and the time required to design and run such a computer program would be very great. Even then the relation of the solutions to the laboratory performance of devices would be questionable because the actual dopant distributions in multiple-implanted and oxidized structures is not well known. The only way to get reliable specific results is by experimented measurement. The purpose of any theoretical analysis should, therefore, be to gain general insight into the physical factors

that limit performance and on their general dependence on the dimensions and other design variables of the structure. This kind of information is useful in arriving at intelligent design choices and in suggesting experimental measurement approaches.

Since the real problem is far too complex to analyze practically, we will develop an admittedly oversimplified model that is easy to formulate as a computer program and requires only modest computation time. The results will not be quantitatively accurate description of the real CCD, but they will show trends that can be expected to be reliable as design parameters and techniques of operation are varied.

2.2 Formulation of Problem

2.2.1 General Formulation

We will begin with a more-or-less complete and general formulation of the charge flow problem and then systematically introduce the series of approximations that leads to our final model.

The effects of electrostatic fields and carrier diffusion can be handled together using the Fermi potential function;

$$\phi_f = V - V_{th} \ln(n/n_o) \quad (1)$$

where V is the actual electrostatic potential, V_{th} the thermal voltage KT/qe , n the density of carriers (electrons), and n_o an arbitrary constant, conveniently chosen in some cases to be the intrinsic carrier concentration $n_i = 1.5 \times 10^{10} \text{cm}^{-3}$. In our analysis we will ignore minority carriers, since in all cases of interest n is much greater than n_i and p .

From the Fermi potential we derive the effective electric field acting on the carriers.

$$\vec{E} = -\vec{\nabla}\phi_f \quad (2)$$

The velocity of the carriers is then given as;

$$\vec{v} = -\mu\vec{E} \quad (3)$$

This can be taken as the definition of the net mobility μ . In practice, the relation between v and ϵ is not linear, especially at high field strengths in the range of $1 \text{ V}/\mu\text{m}$. Figure 2-1 shows experimental values of the net mobility μ_{net} and incremental mobility μ_{incr} for high-quality silicon.

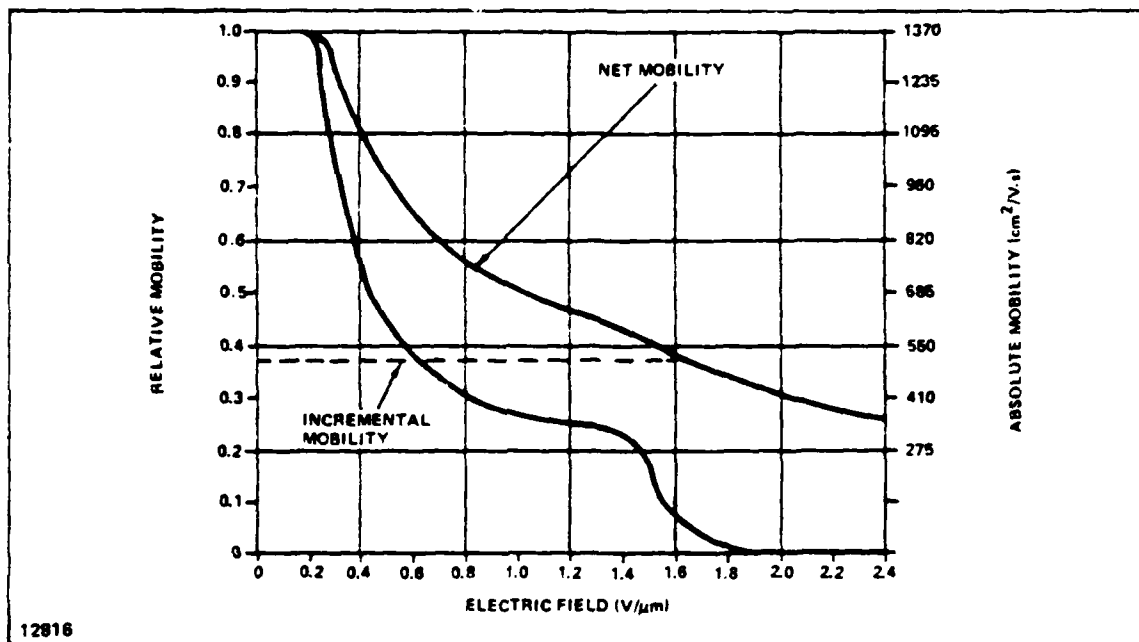


Figure 2-1 - Electric Field versus Mobility in Silicon

$$\mu_{\text{net}} = \frac{v}{\epsilon} \quad (4a)$$

$$\mu_{\text{incr}} = \frac{dv}{d\epsilon} \quad (4b)$$

Note that the net mobility which appears in our equations, falls off more gradually than the incremental mobility. Moreover, in silicon with a low-field mobility of $500 \text{ cm}^2/\text{v}\cdot\text{sec}$, as is more common in CCDs, the curve probably would look like the dashed curve in Figure 2-1. As will be seen in Subsection 3.1 later, when we have very short effective gate lengths ($\sim 1 \mu\text{m}$), we must begin to consider the effect of mobility reduction.

From the carrier velocity given in Equation (3), we derive the flux of carriers \vec{F} as follows:

$$\vec{F} = n\vec{v} = -n\mu\vec{E} = n\mu\nabla\phi_i \quad (5)$$

The continuity equation expresses the fact that if no carriers are spontaneously generated (a reasonable assumption over the short time intervals under consideration here), the change in carrier density is the negative divergence of the flow; that is,

$$\frac{\partial n}{\partial t} = -\nabla \cdot \vec{F} = -\nabla \cdot (\mu n \nabla \phi_i) \quad (6a)$$

$$= -\mu \nabla \cdot n \nabla \phi_i \quad (6b)$$

Equation (6b) holds when μ is constant, as we will assume from this point on. Equation (6a) is fairly generally valid. One significant assumption not yet stated explicitly is that electrodynamic effects are ignored. These include radiation of electromagnetic fields from accelerated charges and magnetic fields induced by time-varying electric fields.

2.2.2 Approximations and Simplifications

2.2.2.1 Limitation to One Dimension

Our first major simplification is to treat all the variables as a function only of the dimension parallel to the direction of charge transport in the CCD channel, which we will call the X-axis. Distributions of carriers into the depth of the structure will be integrated into an effective area concentration. These concentrations will be assumed not to vary across the width of the device. Since the width will typically be 50 μm while the gate lengths and channel depths will be 5 μm or less, this approximation is quite reasonable. Carrier motion in the depth direction will be neglected.

Equations (2) through (6) now take on the form:

$$\frac{\partial n}{\partial t} = - \frac{\partial}{\partial x} \left(\mu n \frac{\partial \phi_f}{\partial x} \right) \quad (7a)$$

$$= - \frac{\mu \partial}{\partial x} \left(n \frac{\partial \phi_f}{\partial x} \right) \quad (7b)$$

Inserting the definition of the Fermi potential from Equation (1), we get:

$$\frac{\partial n}{\partial t} = - \frac{\partial}{\partial x} \left(\mu n \frac{\partial V}{\partial x} - \mu V_{th} \frac{\partial n}{\partial x} \right) \quad (8)$$

The first term represents field-driven flow; the second term represents thermal diffusion ($\mu V_{th} = \mu kT/q_e = D_{th}$ by the Einstein relationship).

2.2.2.2 Local Determination of Potential

We will now make the major assumption that the electrostatic potential $V(x,t)$ at a given point x depends only on the value of the carrier density $n(x,t)$ at that point. This is certainly not always true; the potential in general depends on the charge distribution everywhere. For surface channel devices with the signal charge separated from the gates only by a thin oxide of perhaps $0.1 \mu m$ and with gates on the order of $10 \mu m$ long, the approximation is very good. The approximation becomes less good as the channel becomes more deeply buried ($1/2$ to $1 \mu m$ below the gates) and as the smallest geometrical features of the gates shrink toward $1 \mu m$.

The mathematical consequence of this assumption is the expression:

$$\frac{\partial V}{\partial x} = \frac{\partial V_{ch}}{\partial x} + \frac{\partial V}{\partial n} \frac{\partial n}{\partial x} \quad (9)$$

where V_{ch} is the channel potential when $n = 0$. The second term in Equation (9) accounts for the change in potential caused by the local carrier density. Stated another way, the

first term represents the fringing electric field from the gates and the second term represents the field due to mutual repulsion of the charged carriers. Putting Equation (9) into Equation (8), we get:

$$\frac{\partial n}{\partial t} = - \frac{\partial}{\partial x} \left\{ \mu n \frac{\partial V_{ch}}{\partial x} - \mu \left[V_{th} - n \frac{\partial V}{\partial n} \right] \frac{\partial n}{\partial x} \right\} \quad (10)$$

The term $\mu \left[V_{th} - n \frac{\partial V}{\partial n} \right]$ represents an effective diffusion constant in which the thermal diffusion constant $\mu V_{th} = D_{th}$ is augmented by $\left(\frac{\partial V}{\partial n} \text{ is negative} \right)$ a term proportional to the local carrier concentration.

2.2.2.3 Constant Effective Capacitance

We will now make the relatively minor assumption of a constant effective capacitance in the relationship between V and n. We thus write:

$$V = V_{ch} - \frac{q_e n}{C} \quad (11)$$

and,

$$\frac{\partial V}{\partial n} = - \frac{q_e}{C} \quad (12)$$

This approximation also is very good for surface channel devices where the total effective capacitance is dominated by voltage-independent oxide capacitance. In a buried channel device, the effective capacitance of a nearly empty channel is significantly smaller than that of a nearly full one. One would, on general principles, expect improved performance because the effective diffusion constant at lower carrier concentrations would be larger, and this is when the extra diffusion speed helps the most.

Substituting Equation (12) into Equation (10) we get:

$$\frac{\partial n}{\partial t} = - \frac{\partial}{\partial x} \left\{ \mu n \frac{\partial V_{ch}}{\partial x} - \mu \left[V_{th} + \frac{q_e n}{C} \right] \frac{\partial n}{\partial x} \right\} \quad (13)$$

We can now express the carrier concentrations in terms of the change in channel potential by making the substitution,

$$V_n = \frac{q_e n}{C} \quad (14a)$$

or,

$$n = \frac{C}{q_e} V_n \quad (14b)$$

where we have chosen the symbol V_n to represent the carrier density expressed as an equivalent voltage. Equation (13) can then be converted to a particularly aesthetic form:

$$\frac{\partial}{\partial t} V_n = - \frac{\partial}{\partial x} \left\{ \mu V_n \frac{\partial V_{ch}}{\partial x} - \mu \left[V_{th} + V_n \right] \frac{\partial V_n}{\partial x} \right\} \quad (15)$$

2.2.3 Computer Formulation

We must now convert Equation (15), a second order partial differential equation, to a form suitable for numerical analysis on a digital computer. As with the preceding treatment, we take the simplest and most direct approach. We define the values of V_{ch} and V_n which we will denote as VCH and VN for the computer variables, on an array of x values spaced by DX . The quantity inside the braces of Equation (15) is the flux. It will be denoted as F and defined on an array of x values midway between the points on which VCH and VN are defined.

The derivatives are replaced by finite differences, and the factor $1/DX$ is taken outside the braces. Thus we have:

$$F(I+1/2) = \mu C * \left\{ \left(\frac{VN(I+1) + VN(I)}{2} \right) [VCH(I+1) - VCH(I)] - \left[V_{TH} + \frac{VN(I+1) + VN(I)}{2} \right] [VN(I+1) - VN(I)] \right\} \quad (16)$$

Note that we have used for $VN(I+1/2)$ the average of the values at the two points I and $I+1$ at which VN is defined. Also, since the computer functions with integral indices only,

we actually add 1/2 to the indices of F in Equation (16) and use F(I+1) in place of F(I+1/2). We will continue to use the latter expression here, however, because it makes the relationships of terms clearer.

The solution proceeds as a two step iteration. First, the current values of VN and VCH are used to calculate values of F. Then the values of F are used to get new values for VN using the following Fortran-type equation:

$$VN(I) = VN(I) - \frac{DT}{(DX)^2} \left[F(I+1/2) - F(I-1/2) \right] \quad (17)$$

where DT is the time increment for each step of the iteration. Note that the equation has a scaling factor (DT/DX^2) . This means that as long as the original differential equation remains valid, reducing all distances by a factor of two results in an identical solution evolving four times faster in time. Relative changes in the mobility also can be extracted as part of the scale factor so that doubling the mobility again results in an identical solution but one that evolves two time faster in time.

Boundary conditions must be provided at the first and last points. The specific choice will depend on the problem, but there are two common types. One occurs when the problem area terminates with a high, steep potential barrier. We can represent this case by requiring that the flux F at the boundary be zero. The second common boundary condition occurs when the problem area terminates with a deep, steep potential well. This case is commonly represented by requiring that VN be zero at the boundary. In our formulation of the problem, the boundaries occur between values of VN and at values of F. We therefore handle this case by setting the first value of VN outside the problem area to zero and writing the boundary value of the flux following Equation (16) as shown in Equation (18).

$$F(\text{boundary}) = MU * [VTH + 1/2 VN(\text{boundary})] * VN(\text{boundary}) \quad (18)$$

2.3 Cases Analyzed

Actually getting the computer program written, debugged, and running well was more difficult than expected. In particular, although the iterative procedure is quite simple and straightforward, it does not always converge. Considerable time was required

to learn about the problems that could develop in the calculation and to get the program to trap and/or recover from the errors. With $DX = 0.2 \mu\text{m}$ and $MU = 500 \text{ cm}^2/\text{v-sec}$, time steps no larger than $1/2 \text{ psec}$ and some as small as 1 fsec were required to achieve convergence.

The first case that we chose to look at using the computer program was the equilibration phase of the potential equilibration input technique. We chose this case because it is relatively simple (the channel potentials and boundary conditions are constant in time) and because some published results indicate that this input method begins to degrade in the 50 to 100 MHz range. We were curious to see if the computer program would predict a speed improvement using a $1 \mu\text{m}$ effective gate length of a novel transistor structure that has been developed at Raytheon called an ECMOJ transistor. The channel length of this device is defined by using an undercut etch, hence the acronym ECMOS for "etched channel MOS."

The structure of the problem is shown in Figure 2-2. The source of charge is to the right of the problem area, and the first stage of the CCD is to the left. The problem area itself contains two regions - an input well (IW) and a reference well (RW). The channel

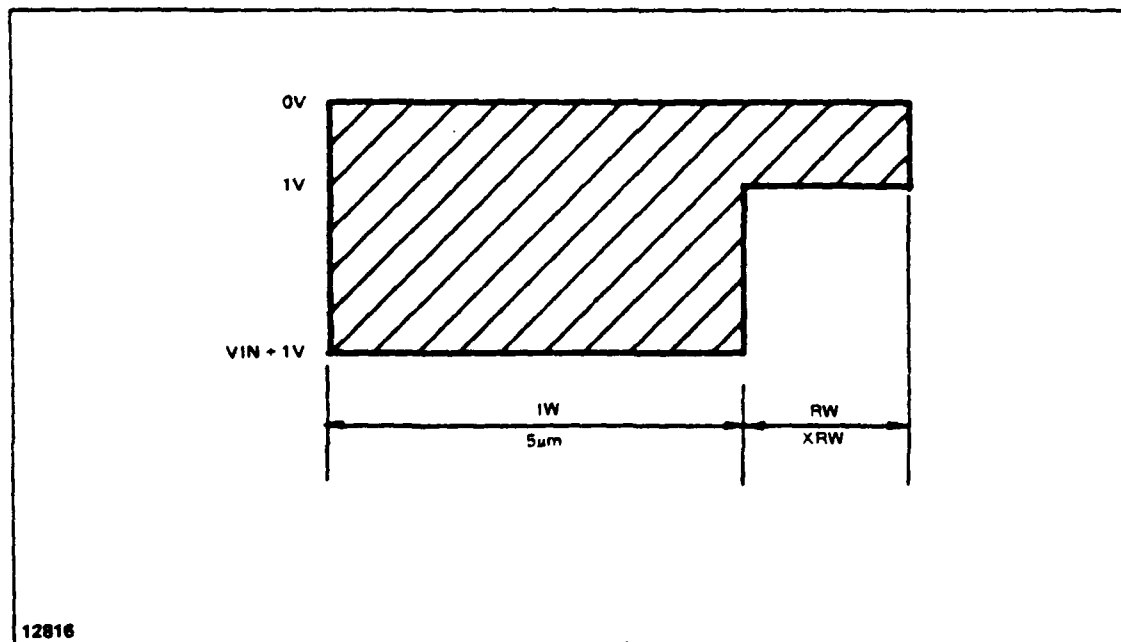


Figure 2-2 - Potential Equilibration Potentials Just Prior to Equilibration

potential in RW is 1 V, and the channel potential in IW is $V_{IN} + 1$ V, where V_{IN} is a variable input voltage. The input well has a width of 5 μm ; the reference region has a variable width XRW. The equilibration phase begins with the entire problem area filled with charge to a Fermi potential of 0v. The left boundary condition is $F=0$; the right boundary condition is a flux corresponding to zero carrier density just outside the problem area.

2.3.1 Test Case

With $V_{IN}=0$ we have the classic charge transfer efficiency problem, for which some closed-form mathematical solutions are available. We used this problem as a test case to verify that the numerical iteration procedure was giving plausible results. The self-field-aided diffusion problem, which we simulated by setting $V_{TH}=0$, has a solution of the form $n(x,t) = n_x(x)n_t(t)$, where the carrier distribution has a shape $n_x(x)$ that does not change in time. The time dependence has the form:

$$\frac{n_t(t)}{n_0} = \frac{1}{1 + \left(\frac{t}{\tau}\right)} \quad (19)$$

which can be rearranged to give:

$$\frac{1}{n_t(t)} = \frac{1}{n_0} \left(1 + \frac{t}{\tau}\right) \quad (20)$$

To test the constancy of the spatial distribution, we first laid the computer-generated graphs of $VN(I)/VN(1)$ over each other. They were indistinguishable for times of 0.25 nsec or more. As a more sensitive check we compared the ratios of peak charge value $VN(1)$ to the total integrated charge. The values for $t=0.5, 1$ and 2 nsec agreed to four decimal places; the value of 0.25 nsec differed by 0.1 percent. The results shown in Figure 2-3 confirm the theoretical time dependence of Equations (19) and (20). For $0.25 \text{ nsec} \leq t \leq 2 \text{ nsec}$ the maximum deviation in $VN(1)$ was 0.0004 V. The time to make the transition from the square distribution at $t=0$ to the time-invariant distribution is about 75 psec.

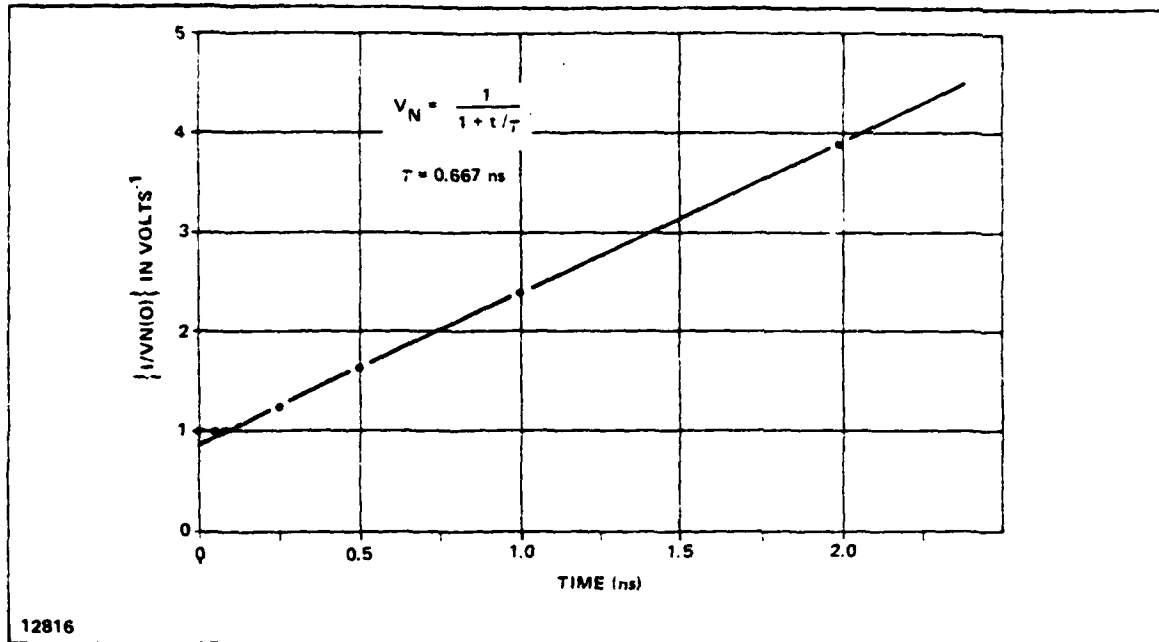


Figure 2-3 - Theoretical Time Dependence of Self-Field-Aided Diffusion

2.3.2 Sample Case

The time evolution of the carrier distribution for a sample case is shown in Figures 2-4 and 2-5. Figure 2-4 shows the distribution of V_N ; Figure 2-5 shows the distribution of the Fermi potential with the constant (see Equation (1)) chosen to give $\phi_F=0$ at $t=0$. The length of the reference gate is $5 \mu\text{m}$ and the value of the input signal 2 V in this case. One sees from these plots that the distribution in the input well is always almost constant. Because of the V_N term in the effective diffusion constant, the effective diffusion in the input well is much larger than that in the reference region. Consequently, the carriers in the input well rearrange rapidly enough to maintain an equipotential distribution.

As a result, for sufficiently large values of V_N (a volt or more, for example), the IW region could be modeled as a single region of width DX with a capacitance that is larger by the ratio X_{IW}/DX , the number of DX intervals in the input region.

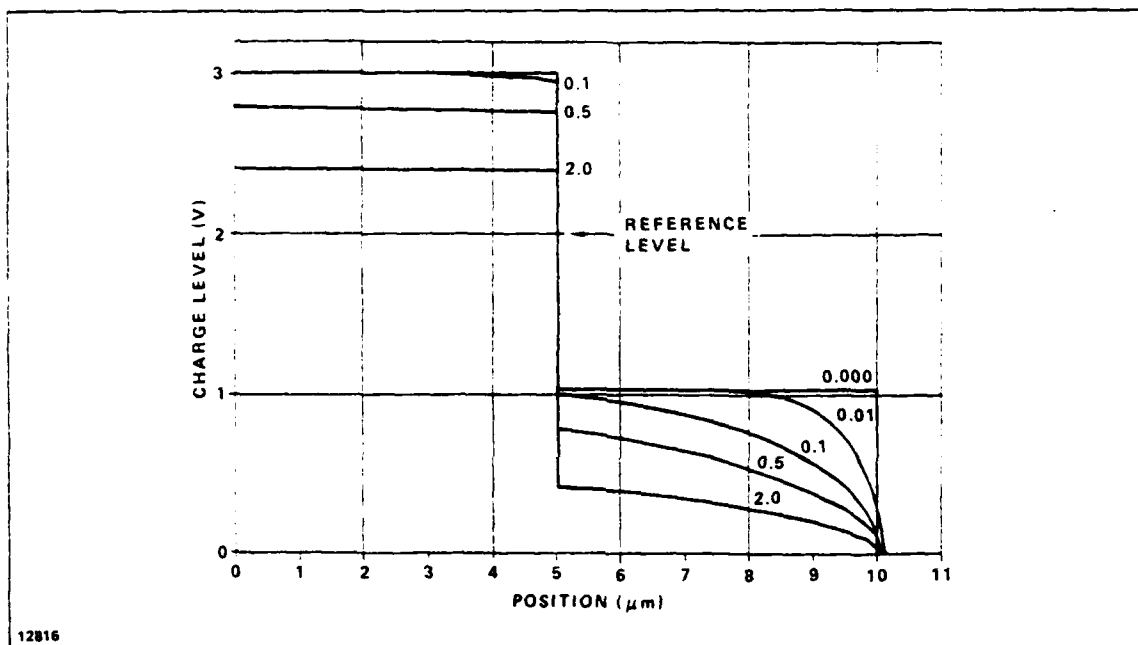
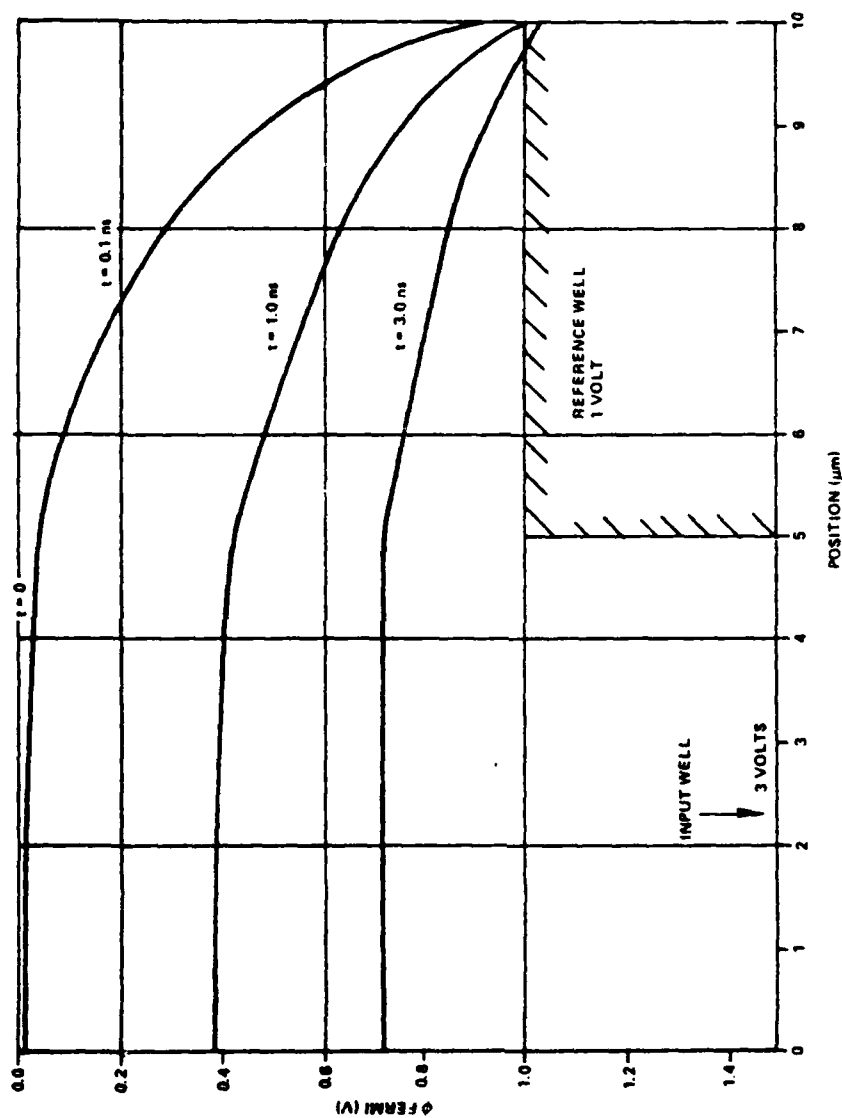


Figure 2-4 - Time Evolution of Charge Level versus Position



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Figure 2-5 - Time Evolution of Fermi Potential versus Position

2.3.3 General Results

The equilibration phase of the potential equilibration input method was studied for a range of values of V_{IN} and values of XRW of 1, 2 and 5 μm . Figure 2-6 shows the results for a 1 μm reference gate at four values of V_{IN} , namely $V_{IN}=0$, 1, 2, and 3 V, for times up to 2.5 nsec. The ordinate shows the amount of charge, expressed in volts, that remains in the input well in excess of the amount that would be there after an infinite equilibration time. Not included in the figure is the excess charge that remains in the reference gate region. When the first stage of the CCD shift register turns on, all of the charge in IW and some of the charge in RW will transfer into the CCD.

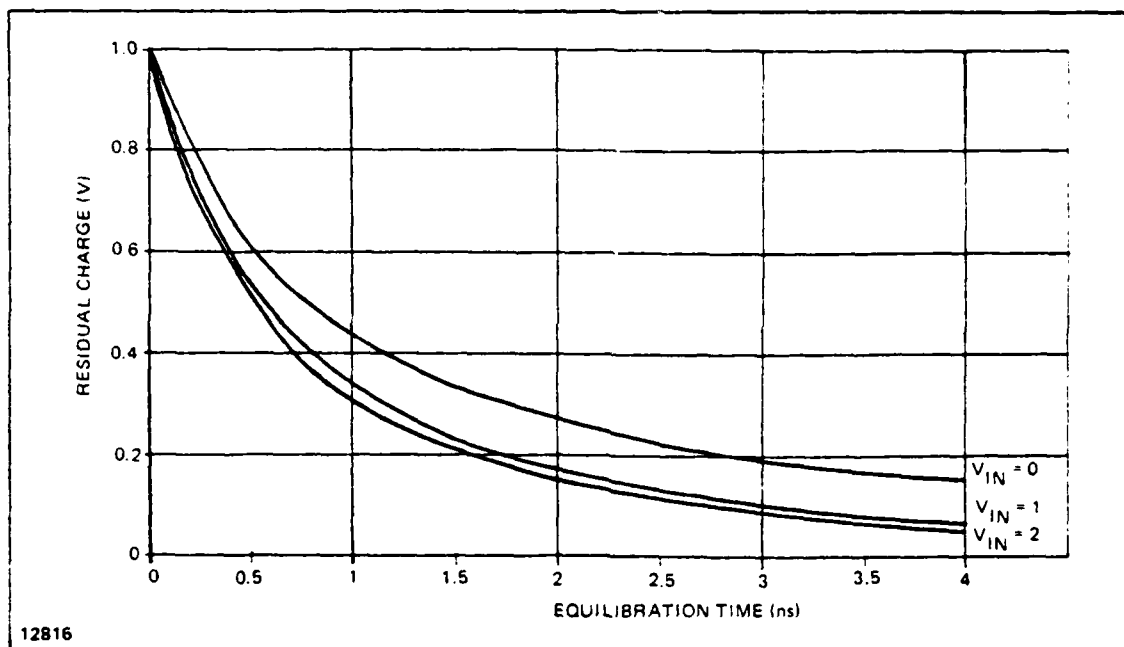


Figure 2-6 - Residual Charge versus Equilibration Time

The excess charge in the input region above the fully equilibrated value has two effects on the performance of the input. First, it changes the relationship between the input signal and the charge injected into the CCD. It always has the effect of introducing what is commonly called a "fat zero." This means that even when the input signal is set to a value to give zero charge, the actual charge will be larger than zero. This reduces the available dynamic range. In addition, if the excess charge does not depend linearly on V_{IN} , a nonlinearity will be introduced into the voltage-to-charge conversion.

The charge versus voltage relationship derived from Figure 2-6 is shown in Figure 2-7 for equilibration times of 0.5 nsec, 1 nsec, 2.5 nsec, and infinity. Only the charge in the input well is included, and it is expressed as the equivalent input voltage for infinite time equilibration. A "least squares straight line" fit reveals that the nonlinearity introduced even at 0.5 nsec is only 1 or 2 percent, not a really significant degradation when one considers that buried channels and fringing effects introduce nonlinearities of this magnitude also.

The second effect of the excess charge on performance is an increase in noise level. When complete equilibration is allowed to occur, only thermal noise is present. Roughly speaking, this results in fluctuations on the order of V_{th} (0.03 V) in the voltage level in the input well. For input signals of 1 V or more, the excess charge has decayed to this level at around 2-1/2 to 4 nsec.

Figure 2-8 shows results similar to those of Figure 2-6 but for a reference gate length of 2 μm . Figure 2-9 shows the result with $V_{IN}=2$ V for a 5 μm reference gate. The curves all have a similar appearance; only the scale of the time axis is changed. Figure 2-10 shows the time required to reach a specified residual charge as a function of reference gate length for an input signal of 2 V. Generally speaking, the speed of the equilibration process increases as L^{-1} .

The linear dependence on L may be surprising at first in view of the general L^2 scaling law mentioned in Subsection 2.2.3. This can be clarified as follows. If we compare two structures, one with a 1 μm reference gate and 5 μm input well and another with a 2 μm reference gate and 10 μm input well, the latter will respond four times more slowly. However, if we keep the input well at 5 μm in both cases, there is relatively only half as much charge that must flow across the reference region. This contributes a two-fold speed increase so that the net dependence on length is L rather than L^2 .

We have operated our current high-speed CCD, which has a 7-1/2 μm reference gate and a 15 μm input well, at speeds up to 60 MHz with good results. The scaled gate shrinkage from 7-1/2 to 5 μm should result in approximately a two-fold speed increase (this change scales as L^2). In addition, provided the drift region that is part of the ECMOS structure does not interfere with the operation of the input, the effective shrinking of the reference gate to about 1 μm should provide an additional factor of five speed improvement. The limit could, therefore, be as high as 0.5 GHz.

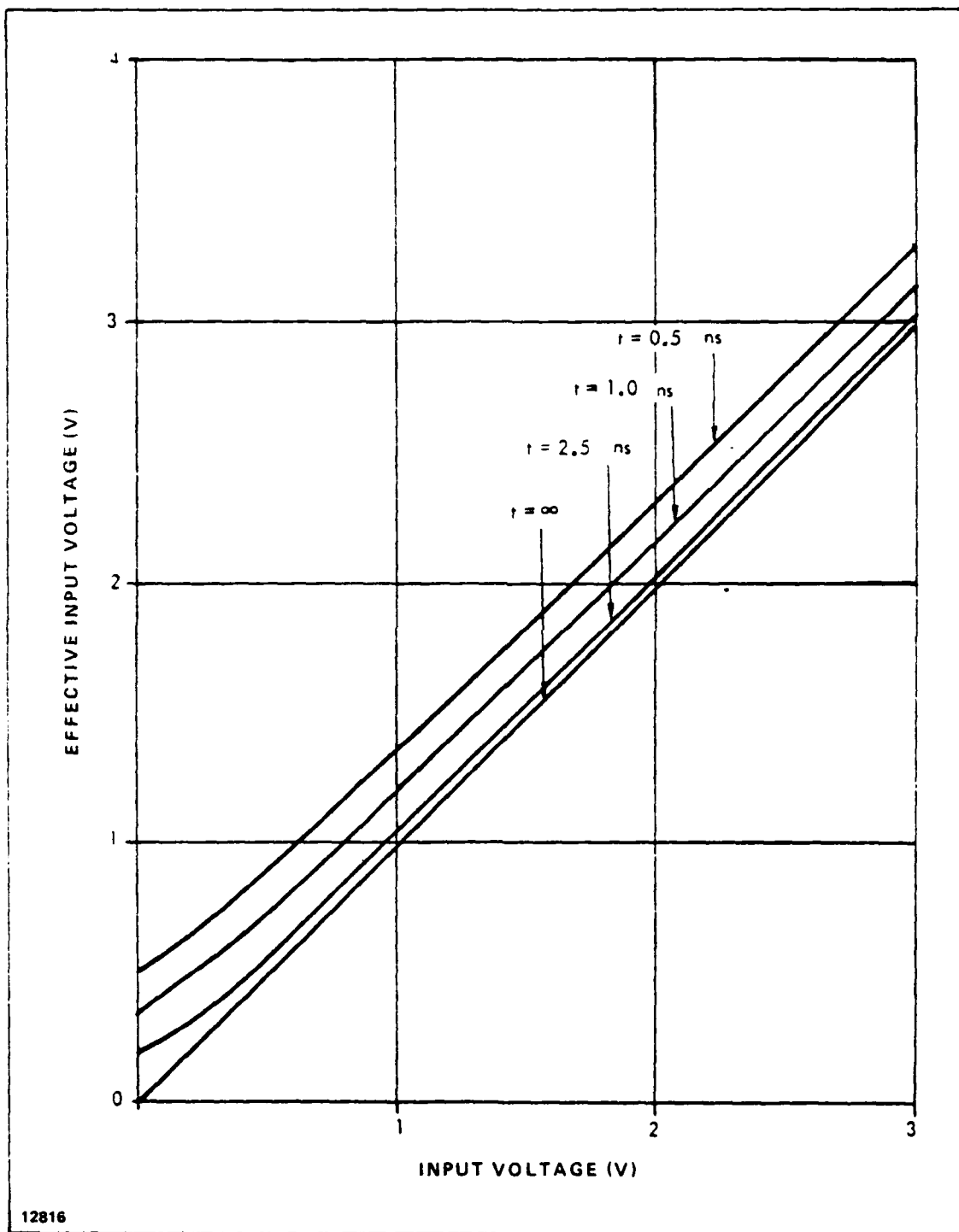


Figure 2-7 - Effective Input Voltage versus Input Voltage

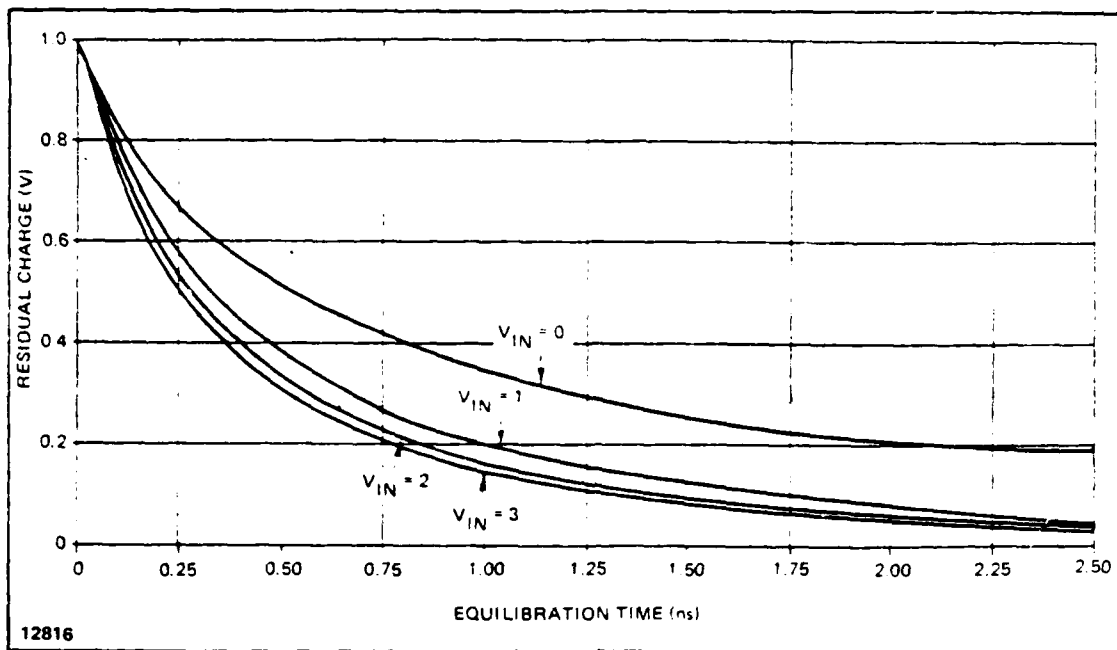


Figure 2-8 - Residual Charge versus Equilibration Time

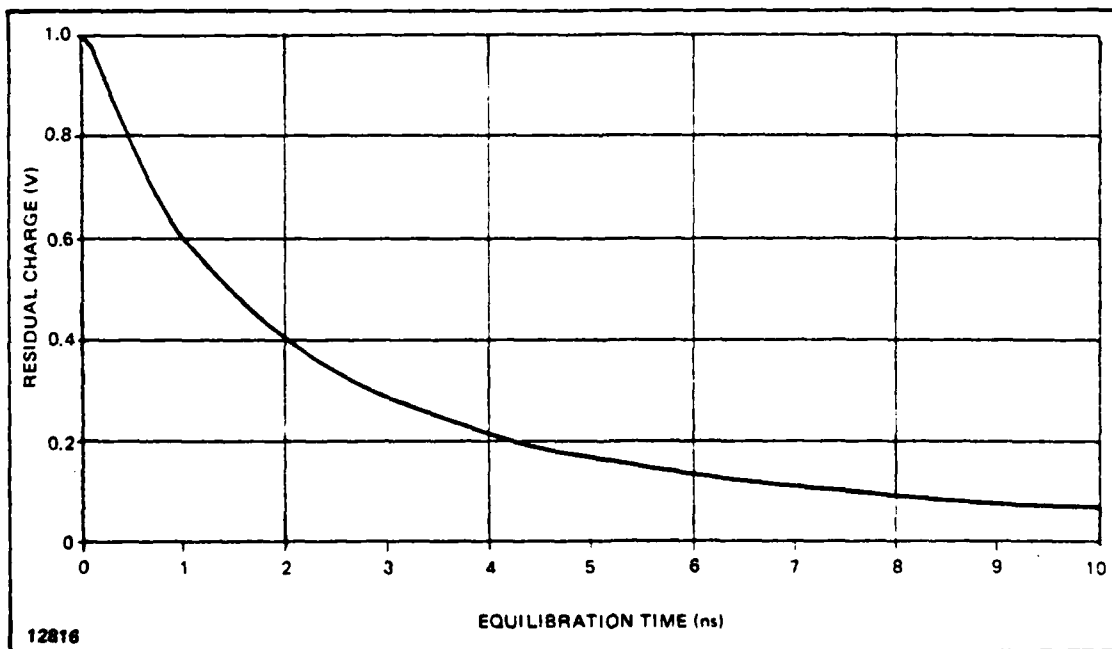


Figure 2-9 - Residual Charge versus Equilibration Time ($V_{IN} = 2$ V)

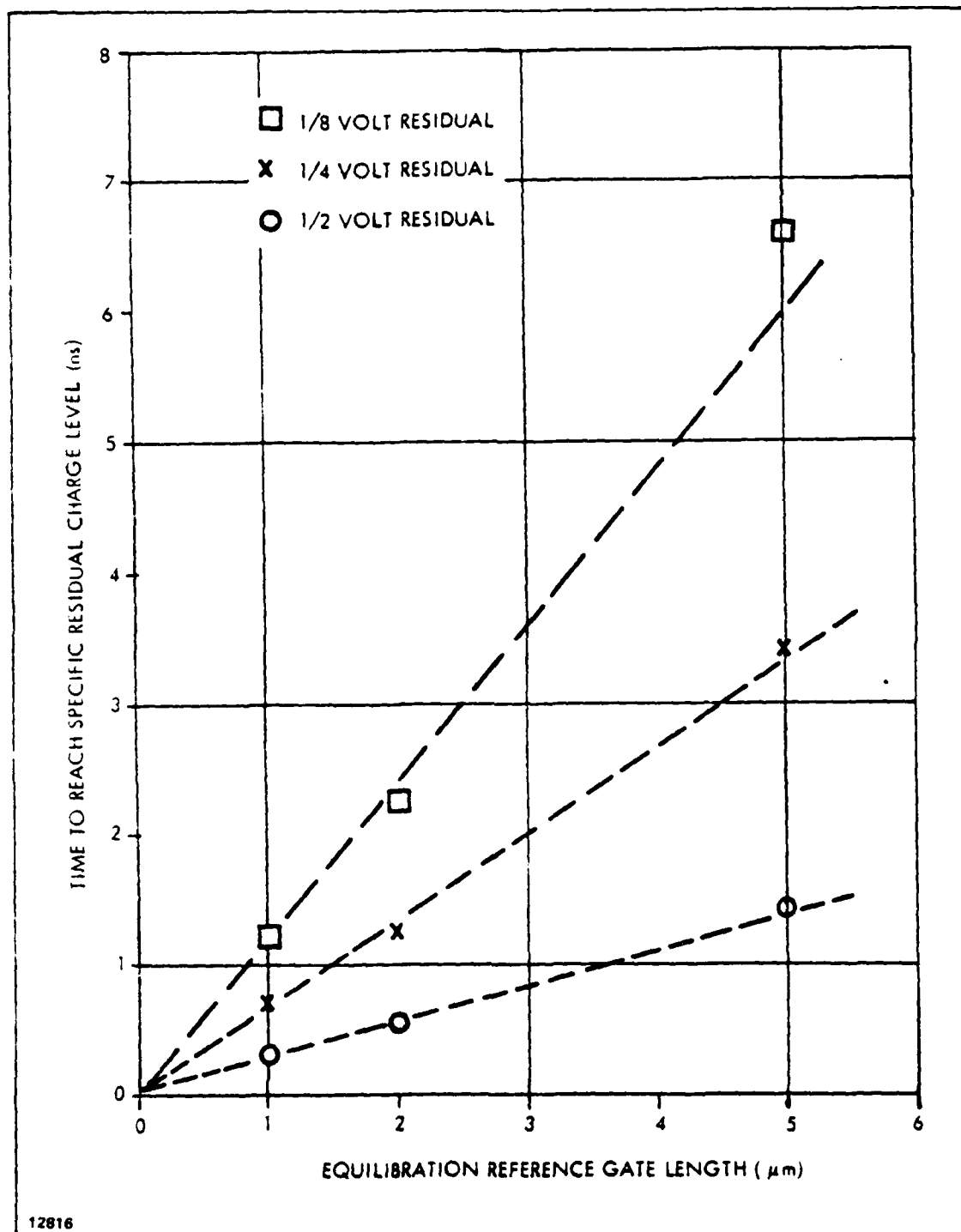


Figure 2-10 - Time to Reach Residual Charge Levels versus Reference Gate Length

2.3.4 Equilibration with the ECMOS Structure

The computer model was extended to include an ECMOS drift region, as shown in Figure 2-11. The purpose of the calculation was to gain insight into the effect of the drift region on the speed of equilibration. The dimensions used as shown in the figure.

Qualitatively, what happens is that first the charge in the drift region flows back into the source. This happens relatively rapidly because of the high carrier density. Once the potential in the part of the drift region that abutts the reference well region has fallen below the potential of the bottom of the reference well, the drift region ceases to be a factor in the equilibration process. Figure 2-12 shows results from the conventional short channel reference gate and for an ECMOS gate with drift region potential well depths of $1v$ and $3v$. There is an initial time delay with the ECMOS gate while the charge in the drift region subsides. Apparently, the charge distribution in the input and reference wells is such, however, that the equilibration process quickly catches up. For $V_D = 1v$, the results are essentially identical after about 1.5 ns; for $V_D = 3v$, less than half a nanosecond is needed to catch up. Clearly, an ECMOS input gate is just as fast and effective as a true short gate.

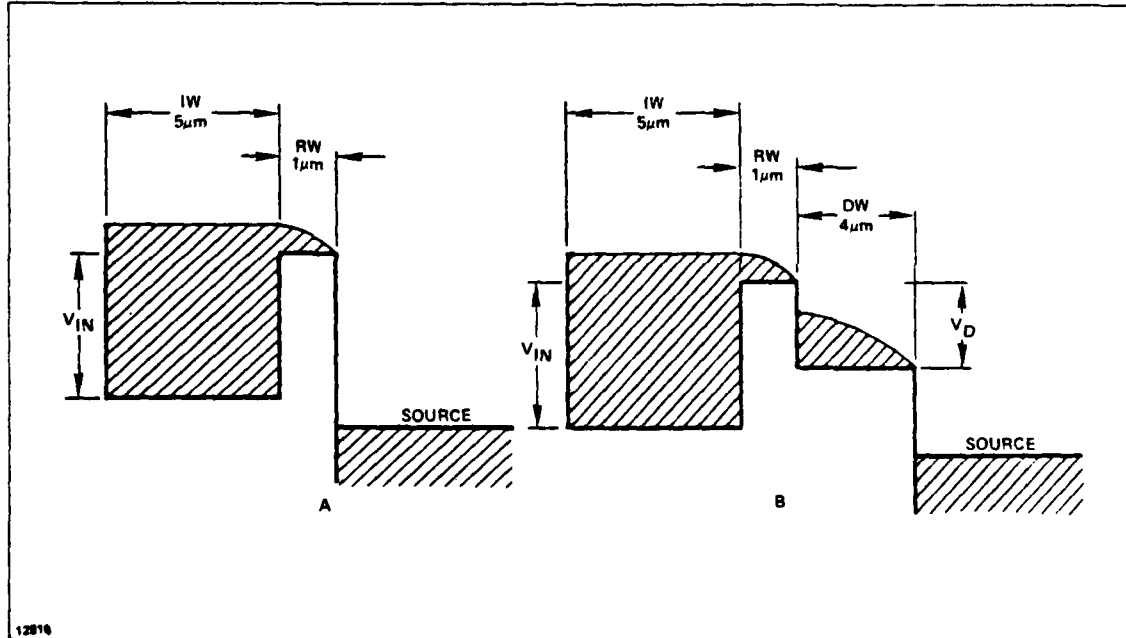


Figure 2-11 - Structures used for Modes of Conventional Type Input (A) and ECMOS Type Input (B)

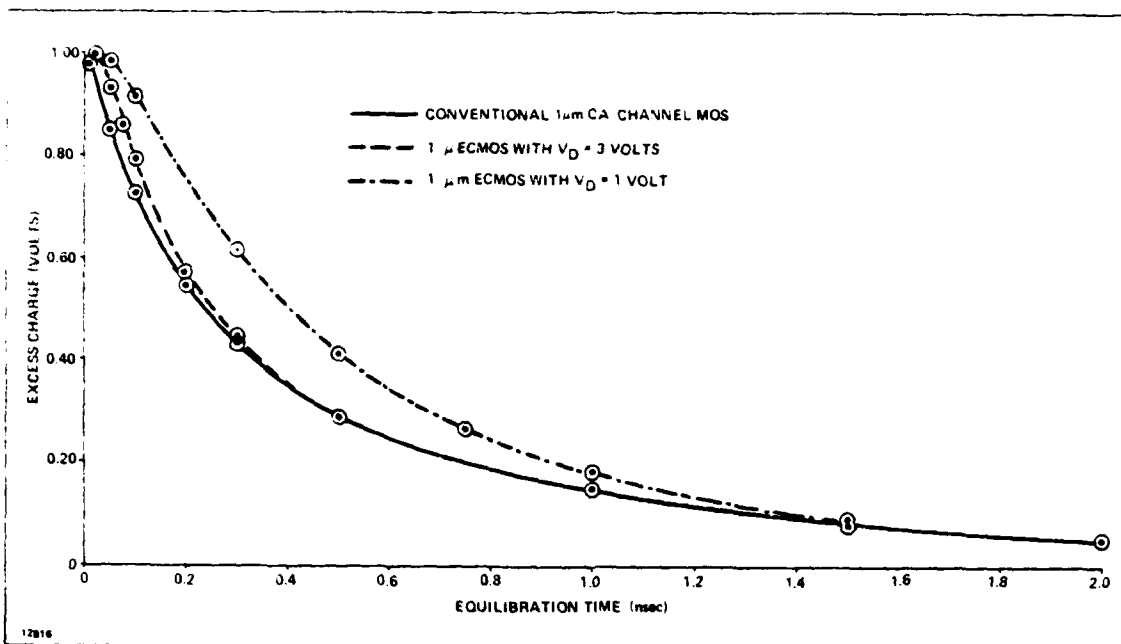


Figure 2-12 - Equilibration Dynamics for ECMOS input Structures Compared to that for Conventional Short-Channel Structures

2.3.5 Election Velocity Saturation

The calculations presented thus far have assumed a constant election mobility regardless of electric field strength. The model was modified to check the effect of election velocity saturation by replacing the carrier velocity by a constant value V_{SAT} whenever μE was larger than V_{SAT} . In general, no effect was found when the actual experimental value of saturation velocity, 10^7 cm/s, was used. To verify that the model did include the effect, some runs were made using a value of velocity only one fifth of the actual velocity. Figure 2-13 shows a typical result. Early in the equilibration, a large charge gradient - and hence electric field - exists in the reference well. This gradient relaxes away quickly, and soon the carrier velocity is no longer saturated. With a velocity saturation value of 10^7 cm/s, a voltage difference of more than 1v must occur across the $1 \mu\text{m}$ reference well before saturation effects will be significant. For a one volt overdrive during the fill phase, this condition will never occur.

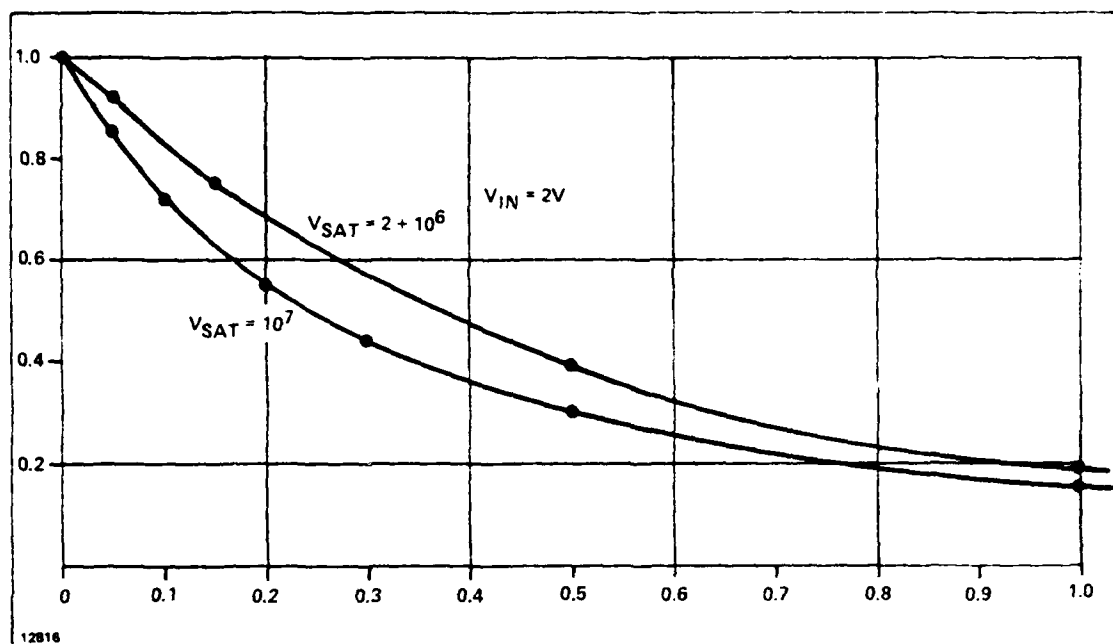


Figure 2-13 - A Significant Velocity Saturation Effect

2.4 Future Theoretical Work

The theoretical work carried out in the contract has consisted of the development of the model and the structure of the computer program, and the computation of the performance of the potential equilibration input technique during the equilibration phase. Future work could examine additional input/output processes and the effects of the approximations used in the model.

2.4.1 Improved ECMOS Model

The model of the ECMOS input in Figure 2-11 was not complete. It included the drift region, which could have been expected possibly to have an effect on performance, but it neglected the fact that the input well would have a part which is a floating diffusion. Figure 2-14 shows the structure which can be compared to Figure 2-11. One would not expect the floating diffusion region to have any significant effect on performance.

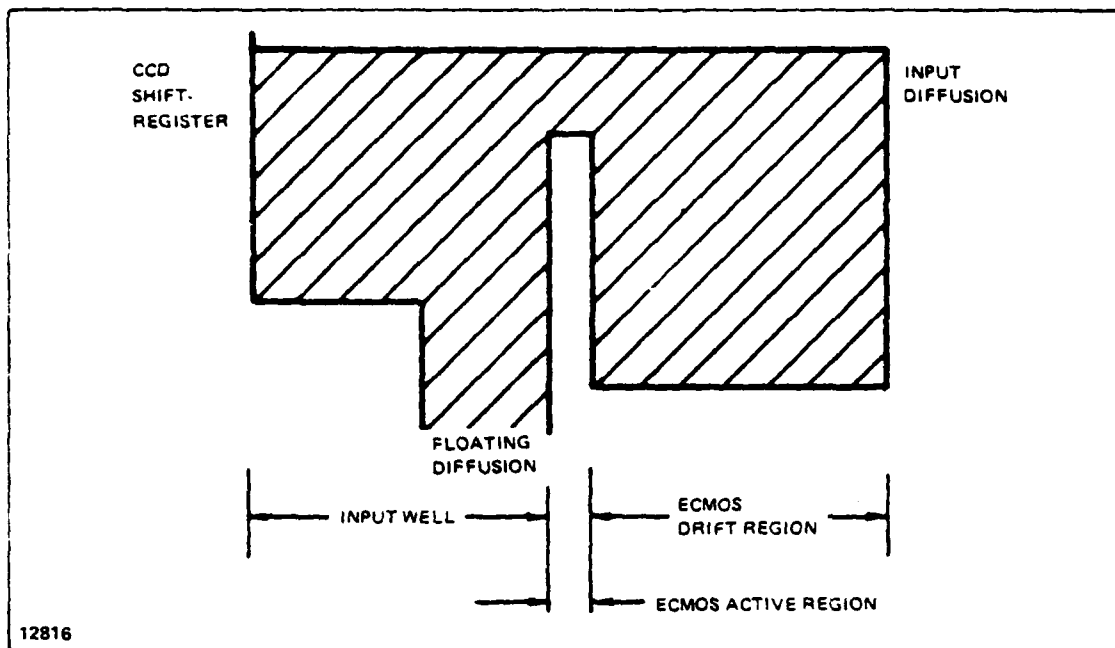


Figure 2-14 - ECMOS Equilibration Structure Potential versus Position

2.4.2 Injection Model

The analysis described above began with an examination of the equilibration phase of the potential equilibration input because this was expected to be the performance-limiting phase. For completeness, the injection phase should also be investigated. The same computer program can be used with only the initial conditions (no charge present) and the boundary condition at the input diode side changed. Both the standard MOS and the ECMOS structure will be considered.

2.4.3 Diode Cutoff Input Model

The diode cutoff technique is expected to be much faster than the potential equilibration technique because the charge is always field-driven. The injection phase is similar to the potential equilibration injection phase. The cutoff phase, however, involves a time-dependent change in the reference gate level from at or below the input well level to above the signal level. The exact way in which the cutoff occurs can be expected to

influence the results. Figure 2-15 shows schematically the kinds of initial intermediate, and final conditions expected with the standard MOD structure. The ECMOS situation is similar but more complex.

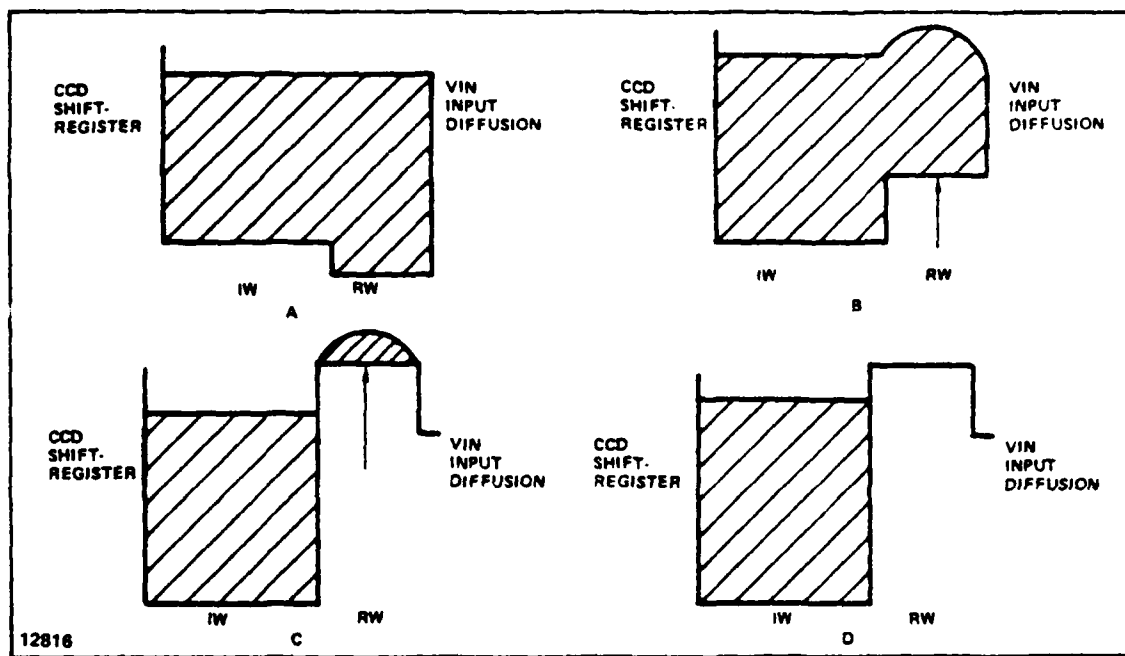


Figure 2-15 - Diode Input Cutoff Method Operating Conditions

2.4.4 Output Structures

The floating-diffusion output structure can be operated in two ways which are similar to the input techniques. The ECMOS output structure is essentially identical to the input structure; the conventional MOS output structure has, in addition, the floating diffusion, which is not present in the conventional MOS input structure. Consequently, the analysis of the output performance should be straightforward.

2.4.5 Effects of Approximations in the Formulation

A number of rather extreme approximations were used in Subsection 2.2.2 to derive the formulation that will be used for the bulk of the theoretical analysis. Some insight into the effects of these approximations can be achieved by treating some cases more carefully.

The simplest improvement to make is to introduce gradations in the values of the zero-charge channel potentials to represent more accurately the effects of fringing fields from the gates to the buried channel.

The effect of carrier velocity saturation and voltage-dependent capacitance can also be examined in a straightforward manner. The nonlocal dependence of electrostatic potential on charge density can be simulated by developing the next order of approximation in which the potential depends *not only on the local charge density but also on the charge density in the neighboring intervals.*

All of these changes will add considerable time to the core computation in the innermost loop. Computer time may become too great to permit exhaustive analyses to be carried out with the more exact formulation, but any significant trends should be revealed from a few key cases.

3. CCD/ECMOS COMPATIBLE TECHNOLOGY

During this phase of the contract, efforts were concentrated on working out design and processing details for the high speed CCD as well as the ECMOS devices to be used for the CCD input, output, output amplifier, and clock driving devices.

The design and fabrication of the high speed CCD delay line closely followed the methods successfully used for the Raytheon 60 MHz CCD. The frequency limitations of this device at 60 MHz are primarily due to the output amplifier response. The frequency response limit imposed by the charge transfer properties of the CCD is substantially higher.

The above conclusion was derived from the fact that the output pulse responses for the 64 stage and 128 stage devices looked identical when clocked at 60 MHz. The excellent high frequency performance of these CCDs was obtained in spite of the fact that the gate length was $7.5\text{ }\mu\text{m}$ for the transfer and storage cells, and the fact that the devices were of the two-phase type. In addition, all gate electrodes were made of polysilicon, with electrode overlaps of $1.25\text{ }\mu\text{m}$. For the purpose of this contract, the channel width of the CCD was reduced from $225\text{ }\mu\text{m}$ to a value in the range $50\text{-}100\text{ }\mu\text{m}$, and cell electrode lengths lowered to $5\text{ }\mu\text{m}$. The gate electrode overlap of $1.25\text{ }\mu\text{m}$ was retained. These changes were implemented to improve high frequency transfer efficiency and reduce the clock capacitance to be driven. A further modification was the use of poly Si-Al or TiW-Al instead of polysilicon for the second layer of gate electrodes (storage cell electrodes). The reduced cell electrode lengths enable the straight 256 stage device to be built with 33 percent shorter overall length.

In the past, the 60 MHz CCDs have been made using an ion implanted guard band to confine the charge to the CCD area in the direction perpendicular to its propagation and to isolate the transistors of the amplifier from each other. This isolation method uses up more space, requires a separate registration step, and leads to higher oxide steps than the so called coplanar or semirox isolation methods.

In the coplanar method, the device to be isolated is first protected by an oxidation mask made up of SiO_2 and Si_3N_4 . The unmasked silicon substrate is etched to a depth about one half the desired field oxide thickness. Boron is then implanted into the surface of the high resistivity P-type silicon to prevent inversion, and field oxide is then grown by thermal oxidation. After this, the masking layer is stripped and the device is formed.

The semirox isolation method is a modification of the coplanar technique which omits the etching of the substrate. As a result, the field oxide forms a step which is approximately one half of its oxide thickness due to the silicon consumed during the thermal oxidation.

The coplanar and semirox isolation methods offer the important advantage that they permit direct contact of field regions to heavily doped regions such as sources and drains of field effect transistors without causing low reverse breakdown voltages. This is not possible with conventional guard band isolation since guard bands are heavily doped and adequate spacing must be provided between them and the source and drain regions.

While ECMOS transistors are readily compatible with the coplanar or semirox isolation, buried channel CCDs using Raytheon's existing process or not. While surface channel CCDs have been fabricated at Raytheon with the coplanar isolation which perform as well as guard banded devices, we have not achieved similar results with buried channel CCDs. It is believed the phosphorus implant used to create the buried channel penetrates the fringe of the isolation region and overcompensates its boron doping. As a consequence, spurious channels have been formed at the boundaries of the CCD buried channels shorting them out.

Although this situation could be corrected by increasing the boron dose in the field, this would also reduce the breakdown voltage of the source and drain regions. For this reason, the new high speed CCD test pattern will utilize coplanar isolation for I/O and transistor structures and guard band isolation for the buried channel CCDs.

3.1 ECMOS Transistor Device Development

Although the work described below was not supported by contract funds, this section is included since ECMOS transistors will be used in the high speed CCD/ECMOS technology under development. The ECMOS transistor offers the main features of the well known D-MOS and V-MOS transistors, namely a short active channel length (of the order of 1 μm) which does not require precision lithography for its fabrication, and a relatively high drain to source breakdown voltage. The main advantages of ECMOS relative to this contract reside in its excellent threshold control, small gate capacitance, and the compatibility of the fabrication procedure with that of CCDs.

The gate capacitance of ECMOS transistors can be relatively small since the portion of the gate covering the drift region can be separated from the substrate by an oxide which is substantially thicker than the gate oxide.

As with D-MOS and V-MOS transistors, a high drain to source breakdown voltage is achieved by employing a drift region in series with the short channel control regions. The purpose of the drift region is to accommodate the voltage difference between the drain voltage and the voltage which can be supported across the active short channel region without punching through. The punch-through voltage increases with the square root of the p-doping concentration in the short channel region and thus increases with the threshold voltage for a given gate oxide thickness.

In order to obtain optimum performance from such a transistor the electric field in the short channel region should approach 10^4 V/cm. At this electric field strength the carrier velocity starts to saturate and close to the minimum possible transit time is achieved. A higher field strength is not advisable since it will not greatly increase carrier velocity and will aggravate short channel effects (drain-voltage dependence of the threshold voltage, and/or punch-through).

The family of drain characteristics with gate voltage as a parameter can be used to determine whether or not a given device attains optimum carrier velocity. As the drift velocity saturates the transconductance reaches its upper limit and becomes independent of the gate voltage. This can be shown as follows in Equations (21) and (22).

$$I_D = \frac{Q}{T} = Q \frac{v_s}{L} = \frac{\epsilon \epsilon_o}{t} (V_G - V_t) (L) (W) \frac{v_s}{L} \quad (21a)$$

$$I_D = \frac{\epsilon \epsilon_o}{t} (V_G - V_t) (v_s) (W) \quad (21b)$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \left(\frac{\epsilon \epsilon_o}{t} \right) (v_s) (W) \quad (22)$$

where

- W = channel width
- L = channel length
- v_s = saturated drift velocity
- T = transit time
- Q = charge induced by $V_G - V_t$
- V_G = gate voltage
- V_t = threshold voltage
- t = thickness of gate oxide

Note in Equation (22) the interesting fact that at velocity saturation the drain current and the transconductance do not depend on the channel length, L . However, a channel length shorter than necessary to achieve velocity saturation can still be important for high frequency operation since it affects the transmit time

$$\left(T_{min} = \frac{L}{v_s} = \frac{C_{ox}}{g_m} \right), \text{ the gate capacitance } \left(C_{ox} = \frac{\epsilon \epsilon_o}{t} (W) (L) \right),$$

and the on-resistance of such a device.

The parameters for an ECMOS test structure can be used to determine whether they operate at close to the carrier velocity limit. Using $t = 7 \times 10^{-6}$ cm, $W = 7.5 \times 10^{-3}$ cm and $(g_m)_{max} = 1.8$ mA/V in Equation (22) we obtain a v_s of 4.75×10^6 cm/sec. This is approximately 80 percent of the saturated velocity (6×10^6 cm/sec) available in bulk silicon.

The following requirements apply concerning the drift region:

- 1) It must conduct sufficiently to permit attainment of an electric field $E_s = 1 \times 10^4$ V/cm in the active channel region
- 2) It must be capable of carrying the current delivered by the short channel region under optimum conditions

Assuming an average drift velocity, v_d for the drift region, the second condition implies Equation (23a) which can be as (23b).

$$\frac{\epsilon \epsilon_o}{t} (V_G - V_t) (W) (L) \left(\frac{v_s}{L} \right) = \frac{\epsilon \epsilon_o}{t_d} (V_G - V_{td}) \quad (23a)$$

$$(W) (L_d) \left(\frac{v_d}{L_d} \right) \quad (23b)$$

$$\frac{V_G - V_{td}}{V_G - V_t} = \left(\frac{t_d}{t} \right) \left(\frac{v_s}{v_d} \right)$$

where

t_d = oxide thickness over the drift region

V_{td} = threshold voltage in the drift region

For practical case one may assume

$$v_d \approx 0.1 v_s, \text{ and } \frac{t_d}{t} \approx 3$$

therefore

$$V_G - V_{td} \approx 30 (V_G - V_t) \quad (24)$$

Consequently, if a gate voltage exceeding V_t by 10 V is desired (corresponding to $I_D/W = 3A/cm$) the threshold voltage for the drift region must be negative and $V_{td} \approx -300$ V. This corresponds to the charge density shown in Equation (25) which corresponds to a density of electronics charge of $N = 2.4 \times 10^{13}/cm^2$.

$$Q/cm^2 = \frac{\epsilon \epsilon_0}{t_d} V_{td} = \frac{4 \times 8.85 \times 10^{-14}}{2.8 \times 10^{-5}} (300) = 3.8 \times 10^{-6} \text{ coul}/cm^2 \quad (25)$$

The charge density calculated in Equation (25) can be located in the oxide as a positive fixed charge, or, more conveniently, can have the form of a donor implant into the surface of the silicon. For both the value of N is rather high to achieve in practice. More easily attainable conditions require that an N of approximately $0.6 \times 10^{12}/cm^2$ be used which will raise v_d to approximately $0.4 v_s$.

Assuming a phosphorus implant is used to obtain the above conditions a dose of $6 \times 10^{12}/cm^2$ and a junction depth of 7×10^{-5} cm, the dopant concentration will be in the order of $8.6 \times 10^{16}/cm^3$.

A boron concentration in excess of this value must then be added to provide threshold control in the short-channel region, and to electrically isolate the source of the ECMOS transistor as shown in Figure 3-3.

Figures 3-1 through 3-3 show three different ECMOS transistor structures under investigation. Structure (Figure 3-1) will be referred to as type A. It relies on the fixed positive charge contained in the oxide covering the drift region L_D to invert the drift region more strongly than the channel region at low gate voltages. The structure shown in Figure 3-2 as type B has a phosphorus implant in most of the drift region.

Structure (Figure 3-3, type C) is the most suitable one of the three for output amplifier applications. In this case the phosphorus doping is implanted during the CCD fabrication sequence and before the device areas are formed. It does not require accurate masking since the excess implant is automatically removed when the silicon surface is etched prior to the formation of the coplanar field oxide.

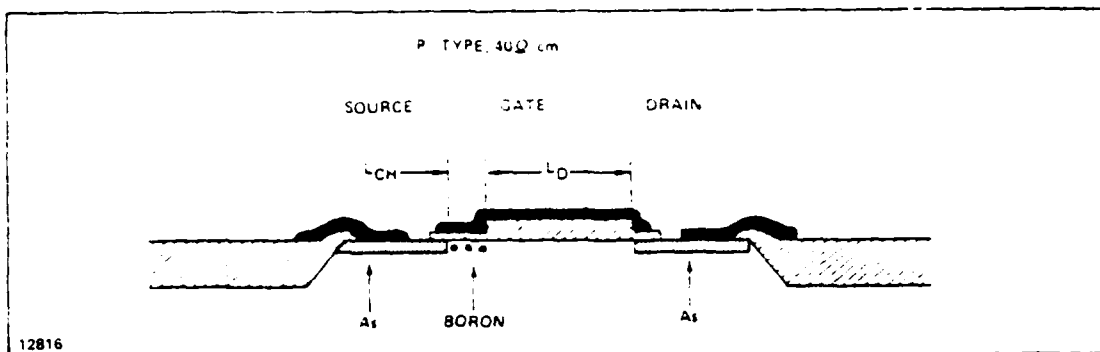


Figure 3-1 - ECMOS Transistor Suitable for Small Gate Voltage Applications

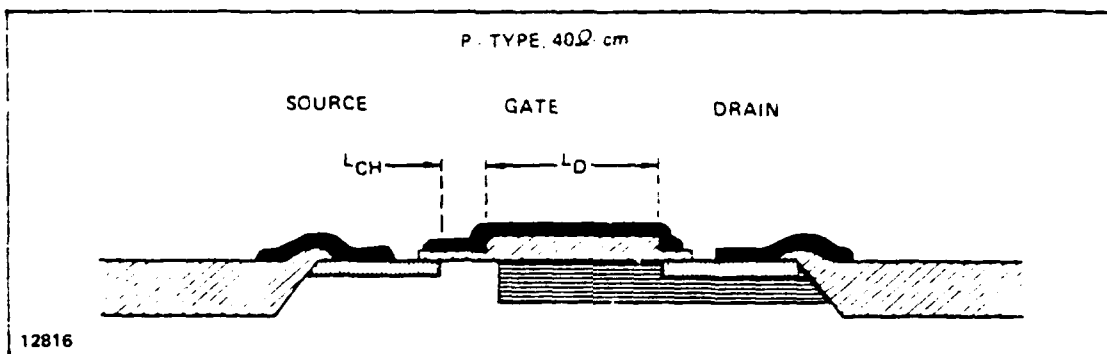


Figure 3-2 - ECMOS Transistor with Reduced On-Resistance Suitable for Large Gate Voltage Applications

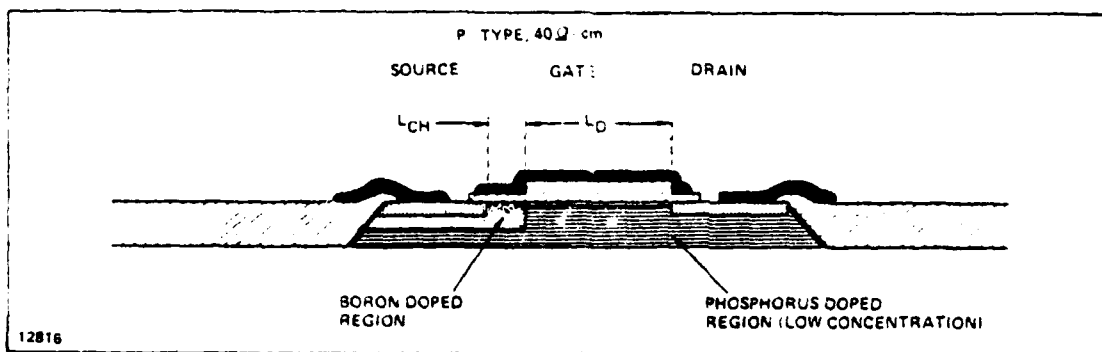


Figure 3-3 - Alternative ECMOS Transistor with Reduced On-Resistance Suitable for Large Gate Voltage Applications

Note that the boron threshold implant serves two functions in the type C structure. It serves to adjust the threshold for the short channel region, and also to diode-isolate the source from the n-type layer. To serve both functions the boron must therefore be driven to a depth exceeding the shallow arsenic-doped source region. Typical S/D families and surface potential v_s gate voltage characteristics are shown in Figures 3-4 through 3-6 for the ECMOS structures shown in Figures 3-1 and 3-3. In all cases, the length of the short channel section was $L = 1 \mu\text{m}$, while the width was $W = 7.5 \mu\text{m}$. For each type of device, the effect of having a drift region of either $L_D = 4 \mu\text{m}$ or $L_D = 6.5 \mu\text{m}$ is also indicated.

As may be expected from the previous discussion, Figures 3-4 and 3-5 show a dramatic change in device characteristics with the length of the drift region. When the phosphorus dose is relatively small ($1 \times 10^{12}/\text{cm}^2$) and $L_D = 6.5 \mu\text{m}$ the electric field at the short channel region is too small to support a saturated carrier velocity. In contrast for a phosphorus dose of $3 \times 10^{12}/\text{cm}^2$, there is much less dependence on L_D since the drift region impedance is much less than that of the short channel region.

3.2 CCD/ECMOS Wafer Fabrication Process Development

The major features of the CCD fabrication method to be utilized can be summarized as follows:

- 1) Ion implantation will be used for most doping steps including isolation, gettering, buried channel, threshold control, and source/drain because of the wide degree of accuracy and reproducibility it affords, as well as the cleanliness it achieves by doping through an oxide and the convenience of using photo-resist as an implantation mask.
- 2) The potential profile for 2 phase buried channel CCDs will be created by the use of two phosphorus implants avoiding the generally used and difficult to control compensation method using phosphorus and boron dopants. In addition, the amount of dopant in the substrate will be minimized.
- 3) Self aligned gates will be created by doping source and drain regions while they are covered by the gate oxide. Thus, undercutting of the gate oxide under the gate electrodes will be avoided.

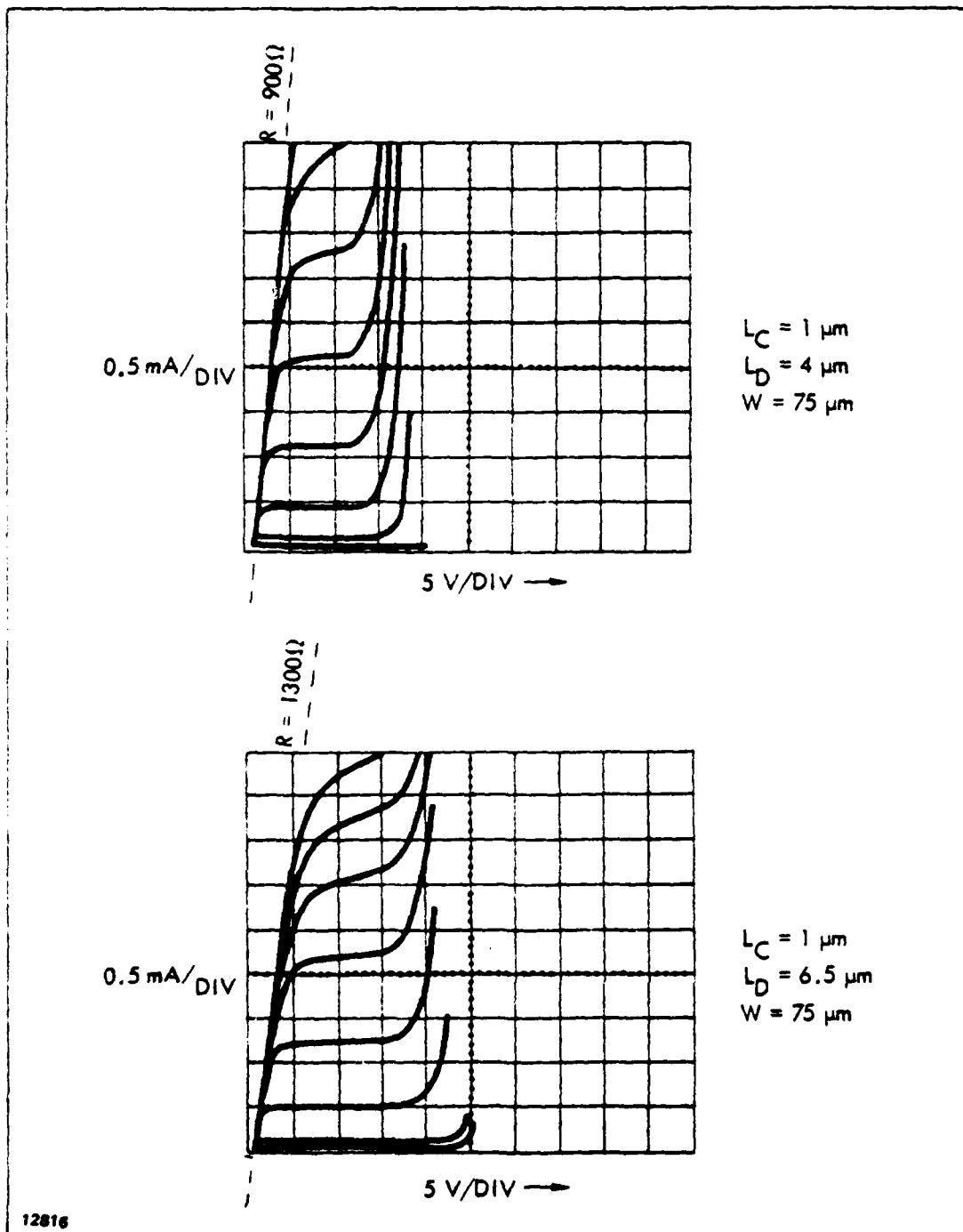
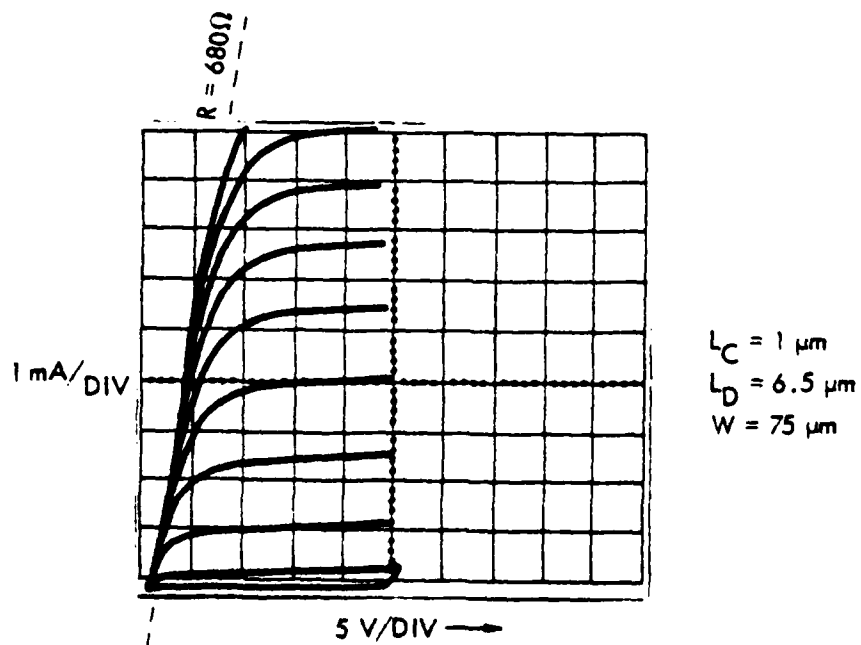
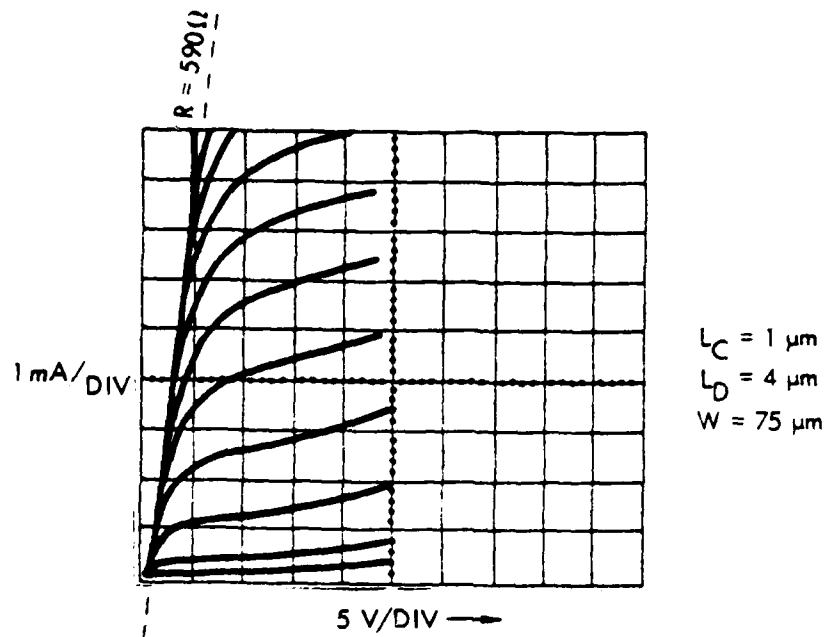


Figure 3-4 - Source/Drain Families of ECMOS Devices (Type A)
with L_D of $4 \mu\text{m}$ and $6.5 \mu\text{m}$



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Figure 3-5 - Source/Drain Families of ECMOS Devices (Type C)
 with $L_D = 4 \mu m$ and $6.5 \mu m$

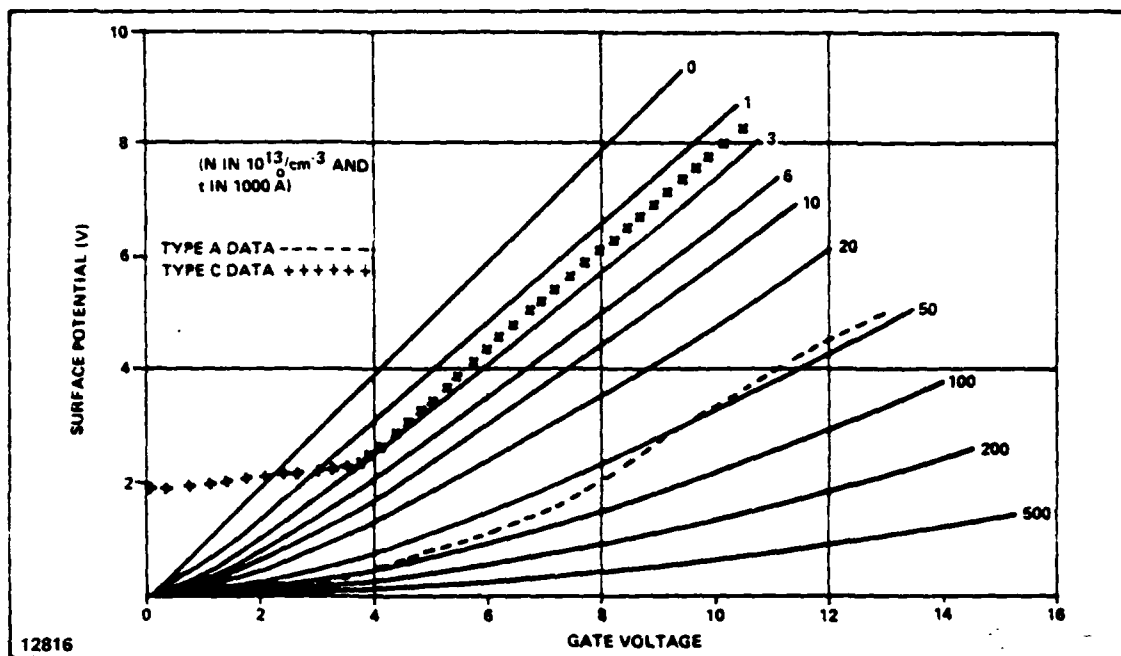


Figure 3-6 - Gate Voltage versus Surface Potential with Nt^2 as a Parameter

- 4) The polysilicon layer will be doped by phosphorus diffusion since this results in a very low sheet resistance ($20 \Omega^2$ for 5000 Å of thickness).
- 5) ECMOS technology will be used for CCD input and output stages to achieve the performance of micron and submicron active channels without loss of charge handling capacity.
- 6) The substrate will be gettered by a BF_2 implant on the back, which also will provide a good back (substrate) contact.
- 7) Polysilicon-aluminum or TiW-Al metallization will be used to provide uniform step coverage and reliable contact to very shallow junctions.
- 8) Mixed coplanar and guard band isolation will be used to optimize the performance and ease of fabrication of the CCD delay line and I/O regions and peripheral transistor circuitry.
- 9) Ultraclean wafer fabrication processing will be used, including the use of polysilicon furnace tubes cleaned with HCl and tight control over the quality of doping and gas supplies.

Figures 3-7 through 3-13 show the processing sequence that will be used. Since the EC MOS transistors used for peripheral circuits may see some treatments different from the EC MOS input and output sections to achieve high current amplifiers, switches, and depletion load devices, a transistor representing an output amplifier stage is shown separately in the figures.

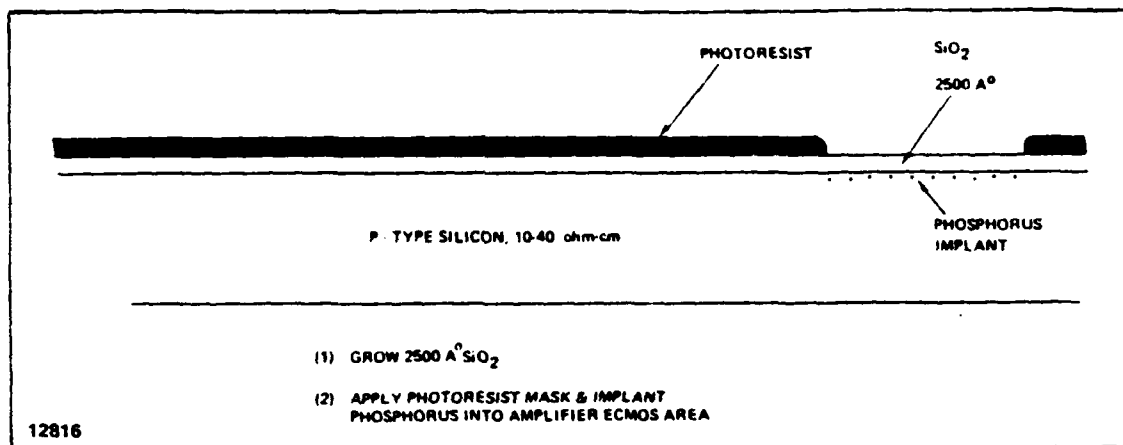


Figure 3-7 - Steps 1 and 2 of CCD/ECMOS Compatible Process

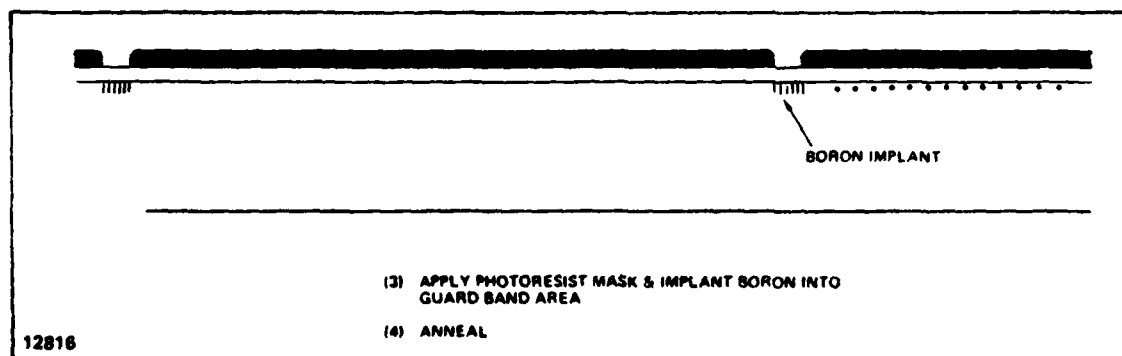


Figure 3-8 - Steps 3 and 4 of CCD/ECMOS Compatible Process

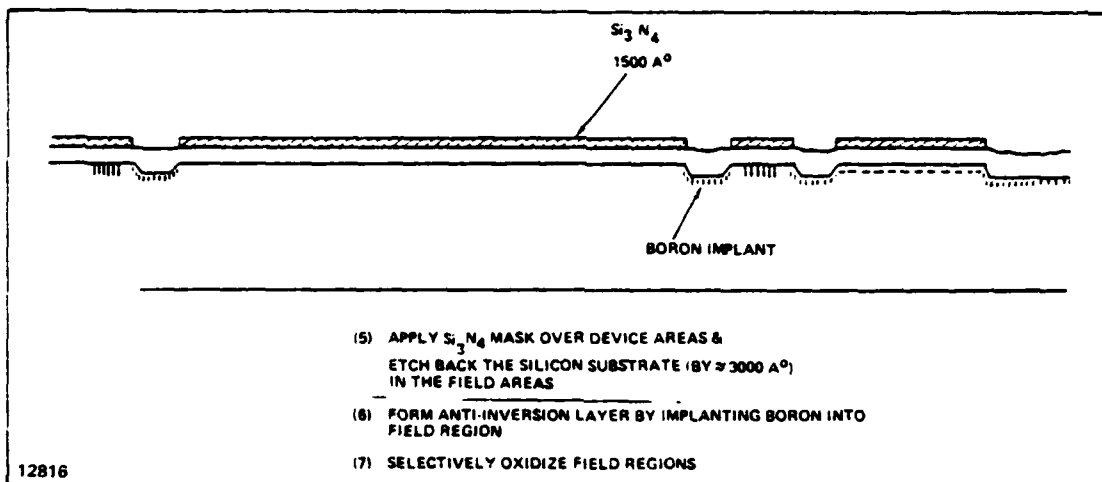


Figure 3-9 - Steps 5 and 6 of CCD/ECMOS Compatible Process

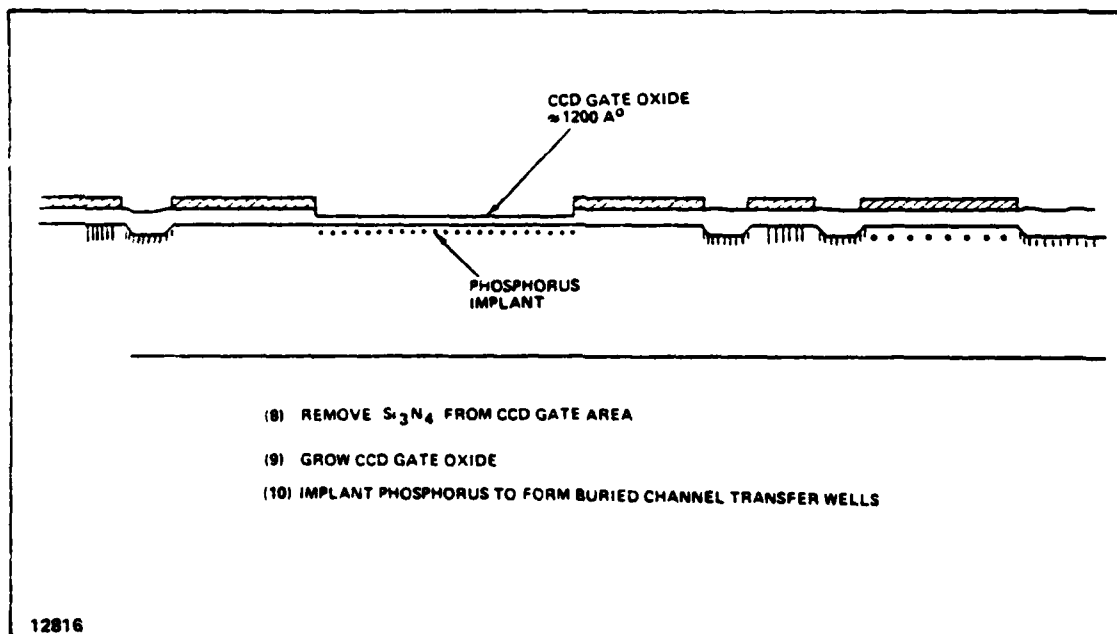


Figure 3-10 - Steps 8 through 10 of CCD/ECMOS Compatible Process

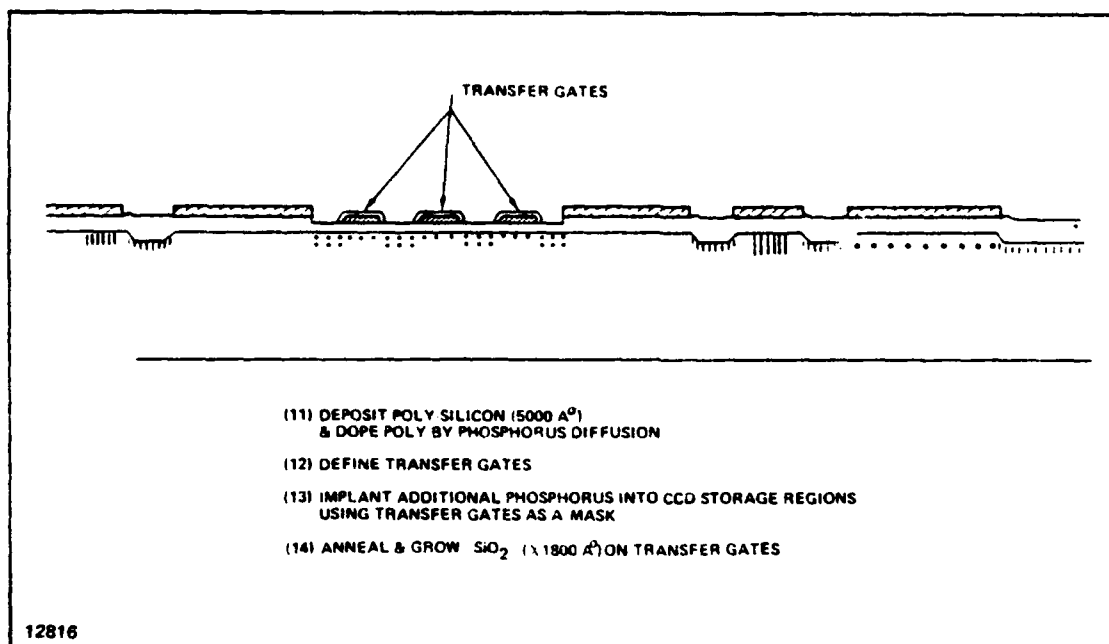


Figure 3-11 - Steps 11 through 14 of CCD/ECMOS Compatible Process

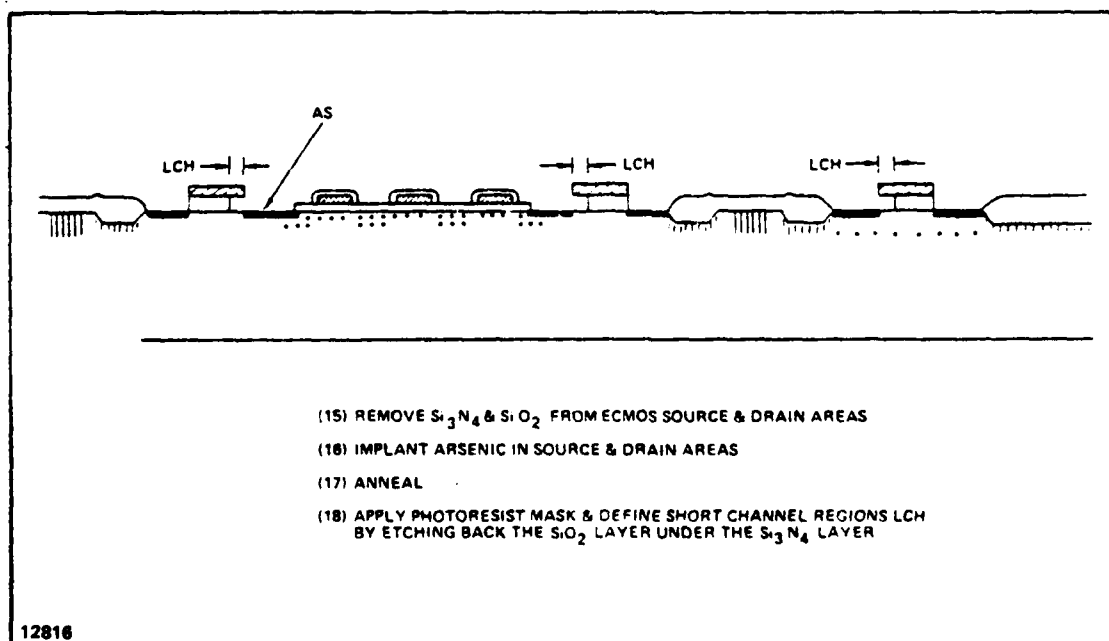


Figure 3-12 - Steps 15 through 18 of CCD/ECMOS Compatible Process

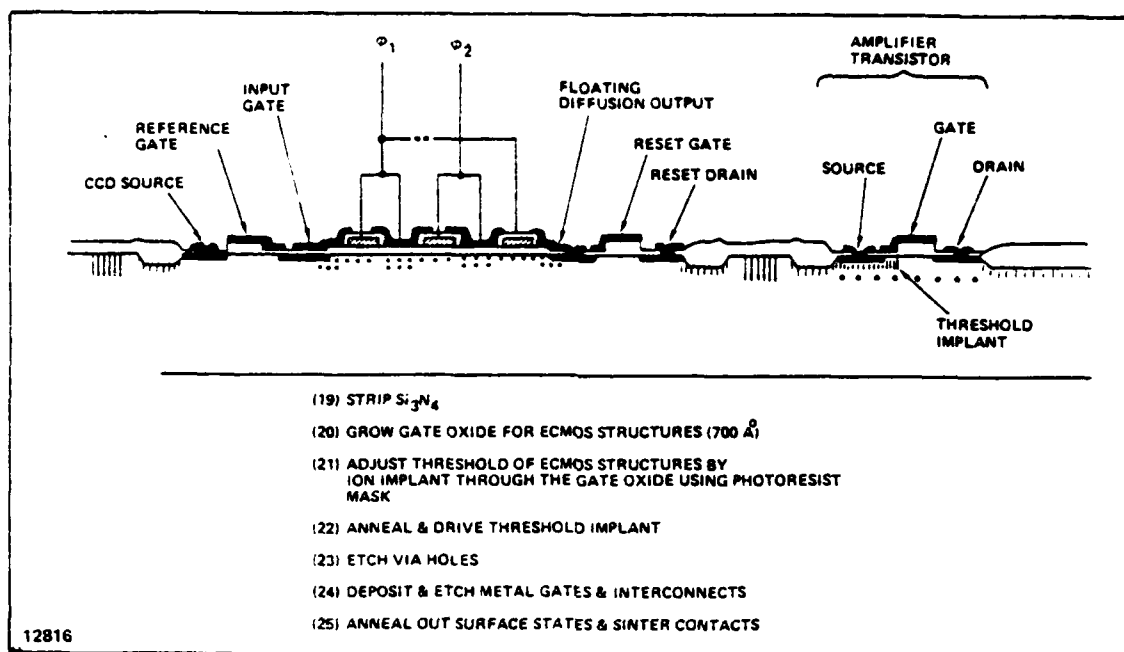


Figure 3-13 - Steps 19 through 25 of CCD/ECMOS Compatible Process

4. HIGH SPEED CCD/ECMOS MASK DESIGN

The proposed advanced high speed CCD technology includes simultaneously fabricated high speed CCD delay lines, higher speed input/output structures and high frequency MOS transistors for both low voltage amplifier and high voltage clock driving applications.

A new mask series was designed to evaluate various approaches to such a technology. The mask series incorporates input/output test structures for the evaluation of conventional high performance MOS and ECMOS gate structures with a variety of channel lengths and widths.

Figure 4-1 shows the functional representation of an ECMOS input/output test structure. Note that it amounts to a high speed CCD with only a single storage well. This pattern will permit the characterization of ECMOS I/O structures for a high speed CCD without the signal degradation caused by multiple transfer and storage stages.

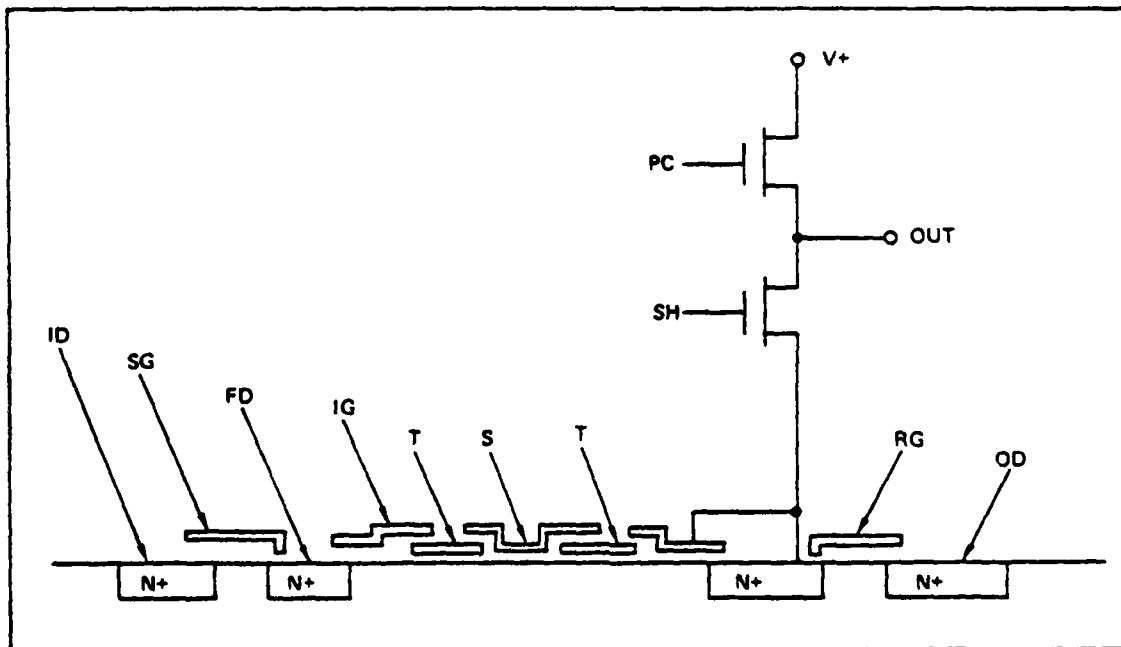


Figure 4-1 - ECMOS Input/Output Structure Functional Diagram

Figure 4-2 is a photograph of the above function using channel widths of 12.5, 25, 50, 100 and 200 μm . The input and output electrodes used are of the ECMOS type and all inputs and outputs are brought to external pads so that they can be evaluated under a variety of bias and signal conditions. The purpose of this group of test patterns is to provide comparison data for five channel widths with respect to harmonic distortion noise, and transfer efficiency at both low and high operating speeds.

Figure 4-3 shows the functional representation of a conventional polysilicon gate input/output test structure.

Figure 4-4 is a photograph of the above function using electrode lengths of 5, 10, and 40 μm and a 200 μm channel width.

In addition to the test cells shown in Figures 4-2 and 4-4, the chip will contain one 256 stage CCD using ECMOS devices for I/O electrodes and output amplifier devices and a second 256 stage CCD using identical 5 μm transfer and storage electrodes but with more conventional I/O and amplifier structures. Performance of a given CCD with conventional polysilicon input/output structures will therefore be directly comparable with the performance of the same CCD using ECMOS I/O and output amplifier structures. Both 256 stage CCDs will use 50 μm wide channels and have 5 μm polysilicon transfer wells and 5 μm wide aluminum storage wells.

It is also desirable to evaluate CCD performance using storage and transfer wells that are not equal in length. In order to evaluate this option, three additional 64 stage CCD delay lines with varying lengths for transfer and storage wells will be provided for this purpose in the mask series.

The chip was divided into the following four sections:

- a) Section A contains a 256 stage CCD with ECMOS drivers, S/H, I/O and amplifier transistor structures.
- b) Section B contains an identical 256 stage CCD, but with drivers, S/H, I/O and amplifier circuitry constructed from conventional self-aligned polygate NMOS transistors.
- c) Section C contains input and output CCD test structures of varying widths and lengths containing both ECMOS and conventional transistors. Section C also contains ring oscillators and individual transistors.

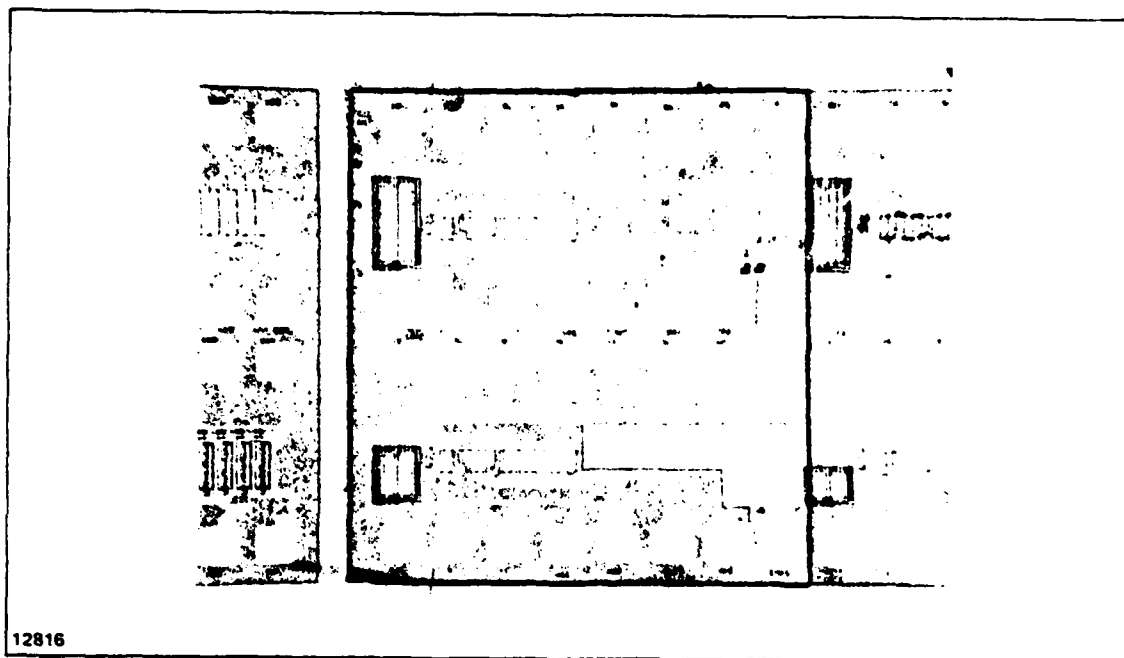


Figure 4-2 - ECMOS Test CCD's $W=100, 200 \mu m$

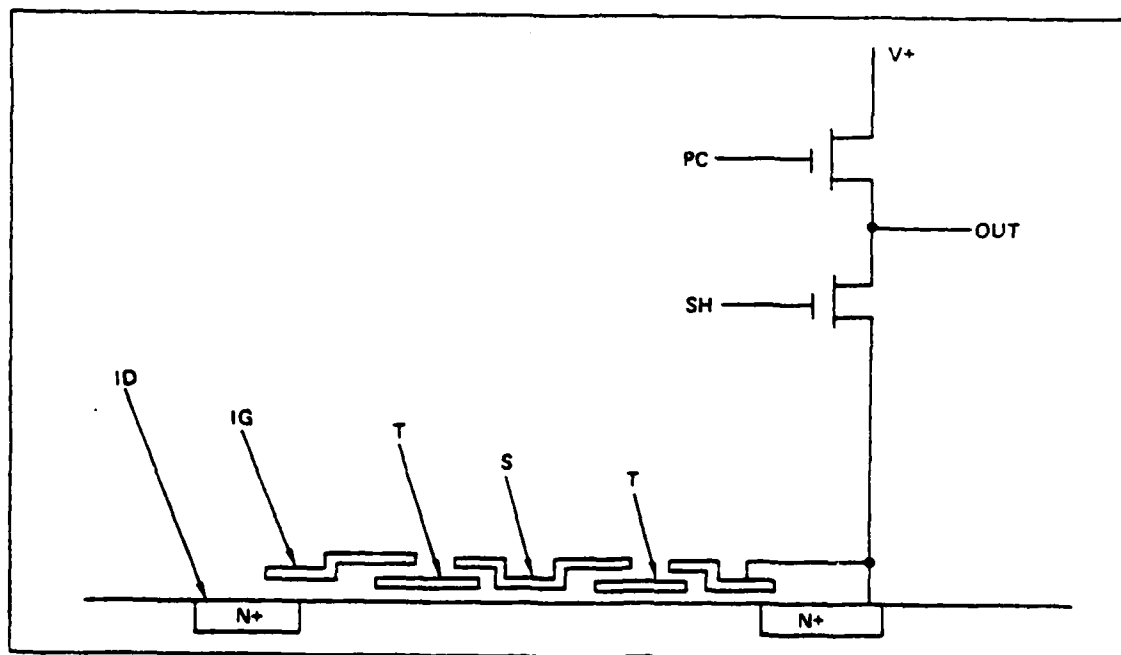


Figure 4-3 - Functional Representation of a Conventional Polysilicon Gate Input/Output Test Structure

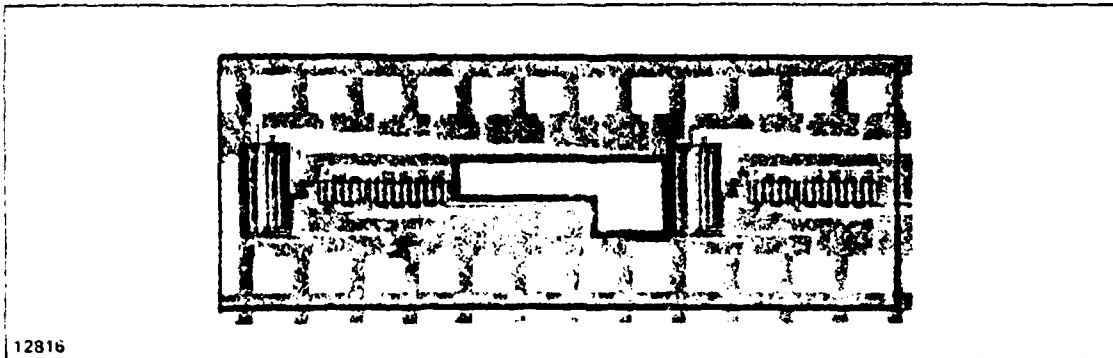


Figure 4-4 - Conventional NMOS

- d) Section D contains a 128 stage CCD without drivers and with conventional devices for input/output structures, S/H and output amplifier. Section D also contains ring oscillators and individual components.

Each of these four sections are bounded with a 4 mil grid and the sections can be scribed and separated individually. The overall chip size is 177.6 x 241.8 mils.

The combined ECMOS, CCD and conventional self-aligned polyprocess requires 12 mask layers through aluminum metallization. Additional options for evaluation of an N+ implant in the ECMOS drift regions of the input and output transistor structures are provided. Metal mask options for the evaluation of drivers and amplifiers independent of the CCD are also provided. Finally, an option for mask defined short channel ($1\frac{1}{4}\mu$) polygate structures is provided. This requires a total of 16 reticles to be generated and stepped into the mask array. Evaluation of the short channel ($1\frac{1}{4}\mu$) conventional devices will require that wafers are processed separately for that purpose. That is, all devices on the self-aligned polysixth mask will be short channel. The N implant under the I/O structures and the individual device metal options will be provided by stepping alternate rows of options into the final masks.

There are a total of 382 bonding pads on the chip, arranged in 10 rows of 4 mil pads on 6 mil centers. Each of the 256 stage CCD arrays are arranged such that the bonding pads will accommodate useage of the same probe card. The remaining 6 rows of bonding pads comprise a random arrangement of input/output and test structures that will require additional probe cards. It is expected that a single curve tracer or DC probing evaluation would be more than adequate to determine whether or not the test devices should be

assembled. Evaluation of high frequency performance will require the assembly of test devices into a package arrangement capable of handling the power and frequency requirements.

In addition to the CCD arrays, ring oscillators, test transistors, resistors and capacitors were added to the chip. The ring oscillators consist of two ECMOS and two standard polygate structures of 19 stages each. An additional two stages are added to each oscillator to buffer the oscillator stages from the output terminal. Both of the ECMOS ring oscillators and the standard ring oscillators are made with depletion loads and with a separate terminal that can be used to connect all the gates of the load devices to a V_{bb} bias terminal. These ring oscillators can be used to provide an indication of the gate delays between ECMOS and standard polysilicon gates.

The capacitors are constructed from the various implants to provide information on the oxides of the process steps. Four point resistors are also provided to monitor the sheet resistance of the implants. Finally, test transistor structures are provided for evaluating the performance of the ECMOS and polygate devices.

5. RESULTS

5.1 Introduction

Unfortunately, two unexplained processing problems prevented the demonstration of operable devices.

The first problem was the disappearance of the nitride layer used for the controlled undercut etching that forms the ECMOS transistors. At no time were the wafers knowingly placed in a nitride etch, but at the critical processing step it was found that the nitride layer had vanished. The conventional type MOS structures, however, were expected to be usable.

The second problem was an oxide problem never seen before. Transistors whose threshold voltages were normally within a volt of zero exhibited threshold voltages of about -5 V or -10 V. Batches of wafers processed together showed some wafers with one value and some with the other. It would appear that the starting material was defective except that the buried channel regions had the threshold characteristics expected. These wafers also exhibited very high dark currents and other peculiarities.

It appeared that the experimental part of this program was going to yield no useful information. The one chance to learn something useful lay in the set of three single-stage test CCD's with different size input gates (see Table 5-1). These devices were included

TABLE 5-1
CCD's WITH DIFFERENT SIZE INPUT GATES

Device Type	Gate Lengths (μm)	
	IG1	IG2
Short (S)	4.0	6.5
Medium (M)	8.5	11.5
Long (L)	13.5	16.5

with the idea that, if the CCD's with high-speed I/O structures were too fast to determine an upper operating speed limit for, one could determine the limit for devices with I/O structures designed to be slow and extrapolate to the performance of the high-speed structures.

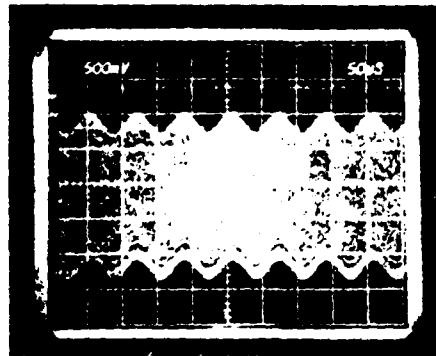
The fabrication difficulties described above took their toll on the small test devices also. Many were totally defective; many operated but with strange characteristics; and all were highly susceptible to gate breakdown. However, some operable devices were obtained and characterized. After the data was analyzed, a surprisingly close agreement was obtained with the theoretical results presented in Section 2.

5.2 Experimental Results

5.2.1 Procedures

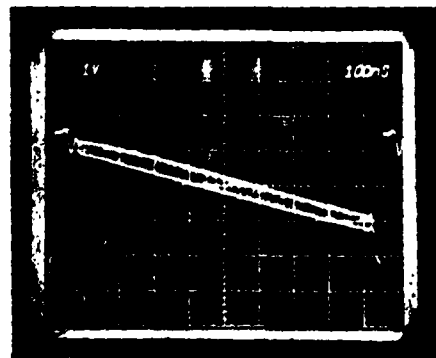
The purpose of the experiments performed on these two devices was to investigate the filling and equilibration (spilling) phases of the potential equilibration input method as a function of the time allowed for each phase. This was done while running the CCD's at a modest overall clock rate of 1 MHz. Thus the output structures of the CCD were operating well within their performance range and were not a limiting factor.

The kind of clock waveforms used are shown in Figure 5-1. The width and position of the sampling pulse (SP) applied to the CCD source were varied. A sample output from the CCD is shown in Figure 5-2. Feedthrough of the various operating pulses can be seen in the output. During the first 100 ns the reset pulse (RP) goes high and back low, O_2 goes high, and O_1 goes low, causing the output signal to appear. To each side of the 800 ns graticule mark, the sampling pulse transitions can be seen (the fill time is about 30 ns). The large transition just past 900 ns is caused by capacitive coupling between O_2 and the floating diffusion. Thus the equilibration time is thus about 100 ns in this photo. The downward ramp in the signal results from extremely high leakage, probably in the reverse-biased floating diffusion.



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Figure 5-1 - CCD Clock Waveforms



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Figure 5-2 - CCD Sample Output

5.2.2 Filling Phase

The filling phase, as expected from theory, is extremely fast, and the experimental results are not easy to interpret precisely. No effects from reducing the length of the sample pulse (SP) could be seen until pulse lengths were very close to the limit set by the equipment.

One problem was to determine the form of the pulse at the package pin of the CCD. The only available tool, an FET probe, had a bandwidth of 500 MHz. Probe distortion is shown in Figure 5-3. Figure 5-3A shows SP applied to the 50 ohm input of a Tektronix 7104 oscilloscope with 7A29 vertical amplifier plug-in (BW = 1 GHz). Figure 5-3B shows what the FET probe saw when SP was terminated with a 50 ohm pad. The apparent pulse amplitude is in error. The apparent pulse length is correct, however.

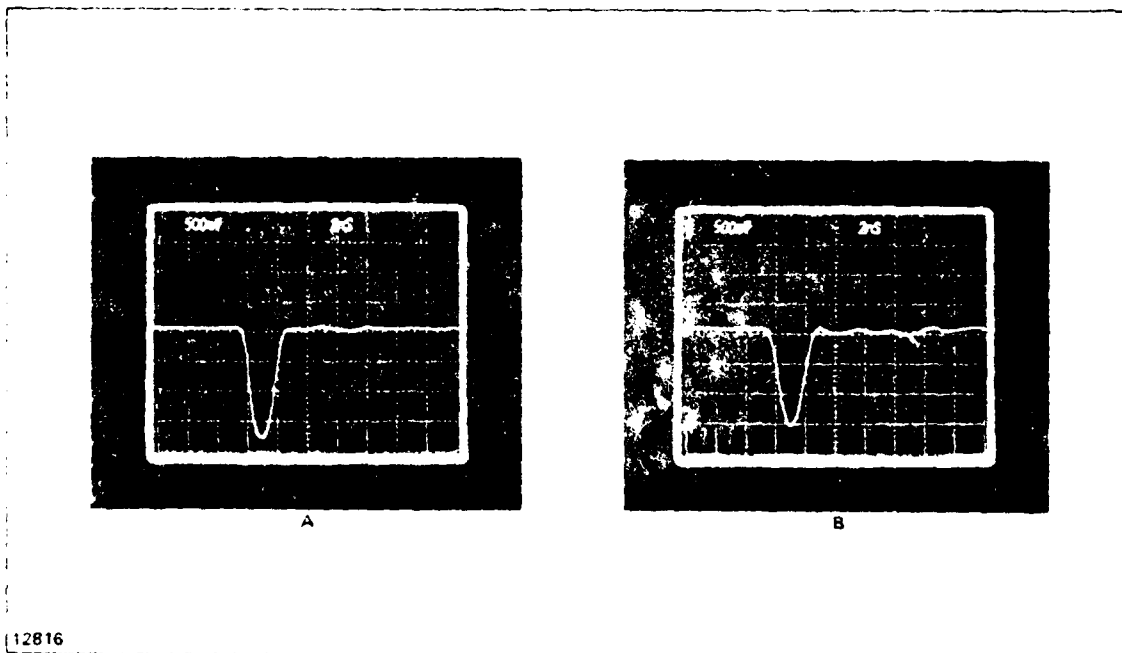


Figure 5-3 - Minimum Length Sample Pulses

The dependence of the filling behavior on SP length depends critically on the exact conditions. Figure 5-4 shows the output signal and its spectrum for a sine wave input when the sample pulse caused filling to occur for 6 ns. The CCD was of type L. Almost no change was observed as the fill time was reduced to 2.8 ns (Figure 5-5A). At 2.4 ns (Figure 5-5B) distortion can be seen. The output is unchanged for small signal packets (higher output voltage), but there is not enough time to provide more than a half-full-well when the input signal corresponds to a large packet. Some or all of the change may have been the result of an amplitude change in SP in going from 2.8 ns to 2.4 ns. Reducing the SP low level by 0.2 V restored the signal nearly to its original form.

Figures 5-6 and 5-7 show another set of results with pulse lengths of 2.3 ns and 12 ns. The change in output signal is so small that it can be seen only with the spectrum analyzer.

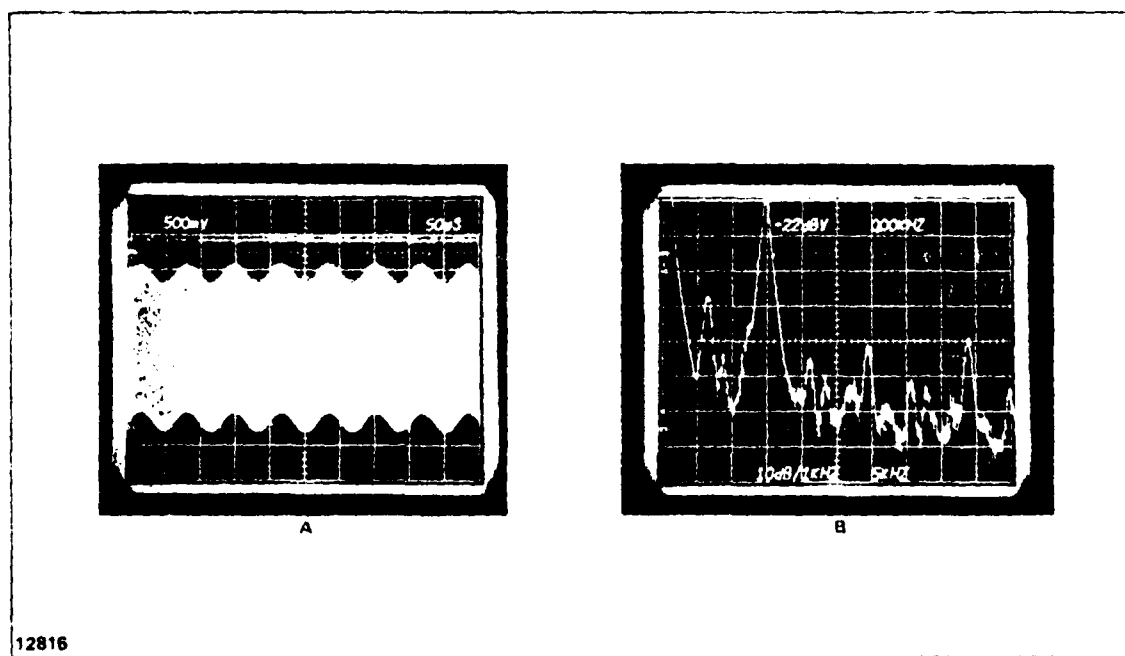


Figure 5-4 - Output for a 6 ns Sampling Pulse. A) Waveform; B) Spectrum.

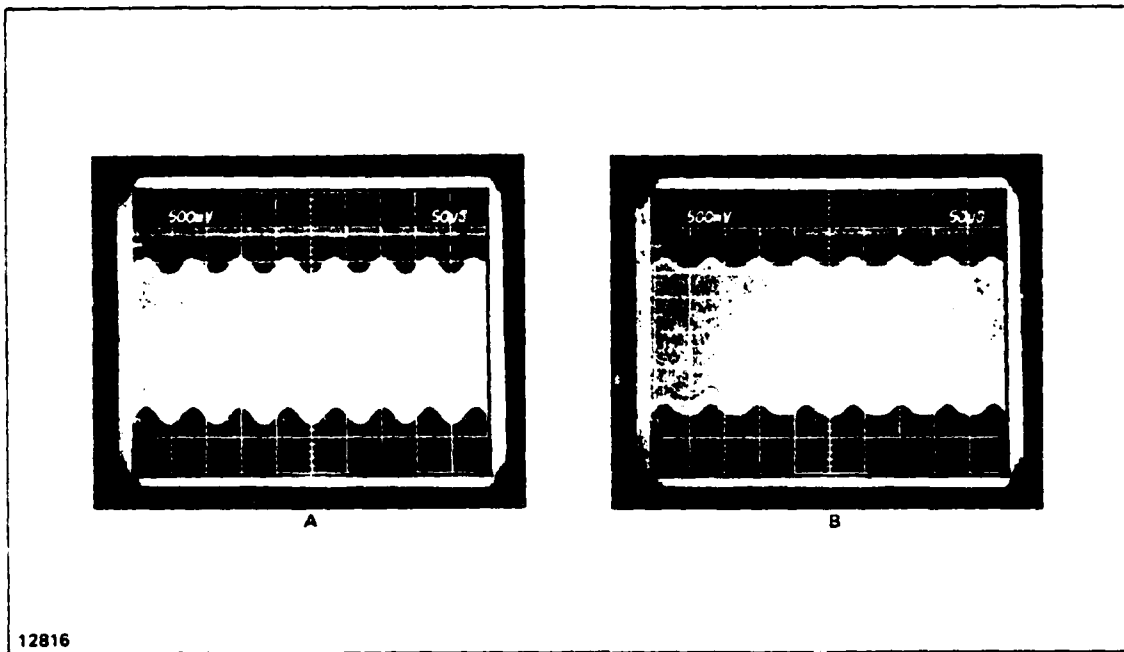


Figure 5-5 - Output Waveforms for SP Reduced to 2.8 ns A) and 2.4 ns B)

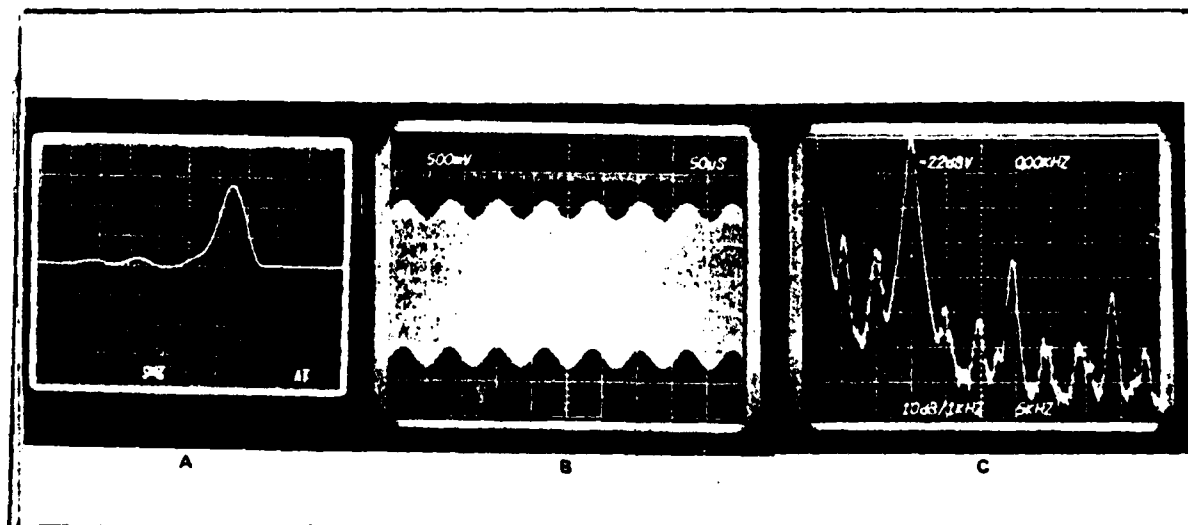


Figure 5-6 - Another Set of Results With SP at 2.3 ns. The Sample Pulse is Shown in A), the Output Signal in B), and the Spectrum is C)

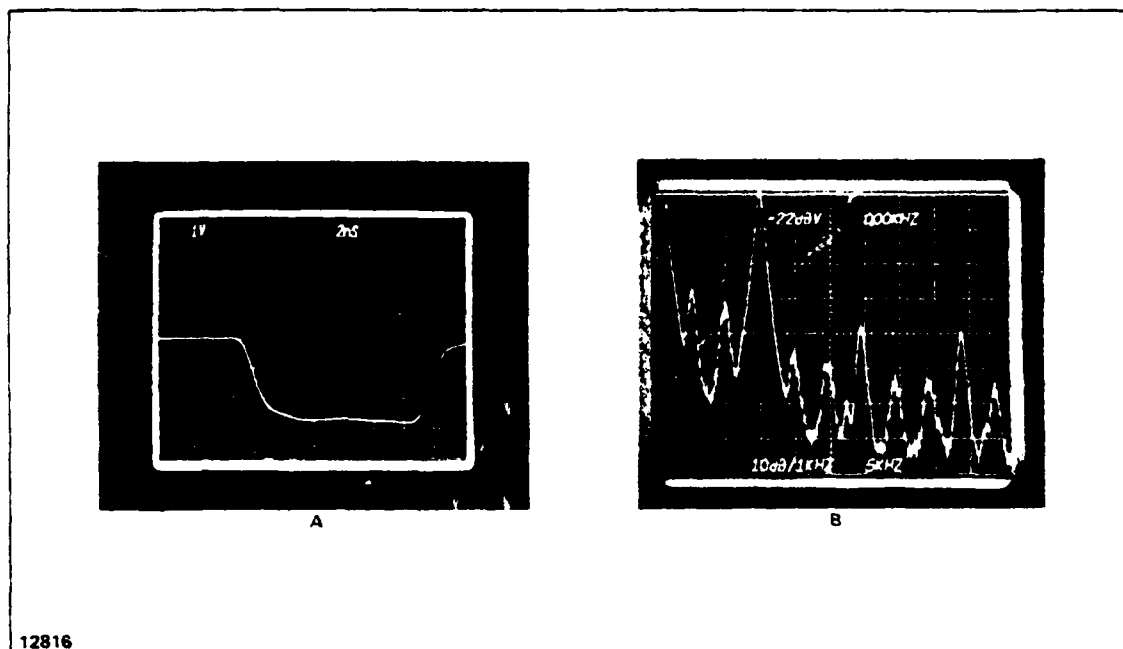


Figure 5-7 - Change in Result when SP was Increased to 12 ns. The Sampling Pulse is Shown in A) and the Spectrum in B)

5.2.3 Equilibration Phase

The dynamics of the equilibration phase of the potential equilibration input technique were studied by using a fixed, 20 ns-long sampling pulse which ended a variable amount of time before 0_1 turned on and transferred the charge into the CCD. Figure 5-8 shows results for a medium length gate CCD with equilibration times of 110 ns and 5 ns. At first glance the pair of photos seems the same as those in Figure 5-5. Careful examination, however, reveals a critical difference between the two distorted outputs. In Figure 5-8B the entire output signal has shifted downward (more electrons in all the charge pockets) until saturation of the CCD transfer wells occurred. In Figure 5-5 the undistorted part of the output is unchanged. The explanation is that in Figure 5-8B the input well under IG_2 , which is overfilled during the sampling pulse, has not had time to equilibrate.

At this point a very important result was observed. A slight reduction in the DC component of the signal on IG_2 caused the output signal to be restored to its original form, as shown in Figure 5-9. The spectra corresponding to the signals in

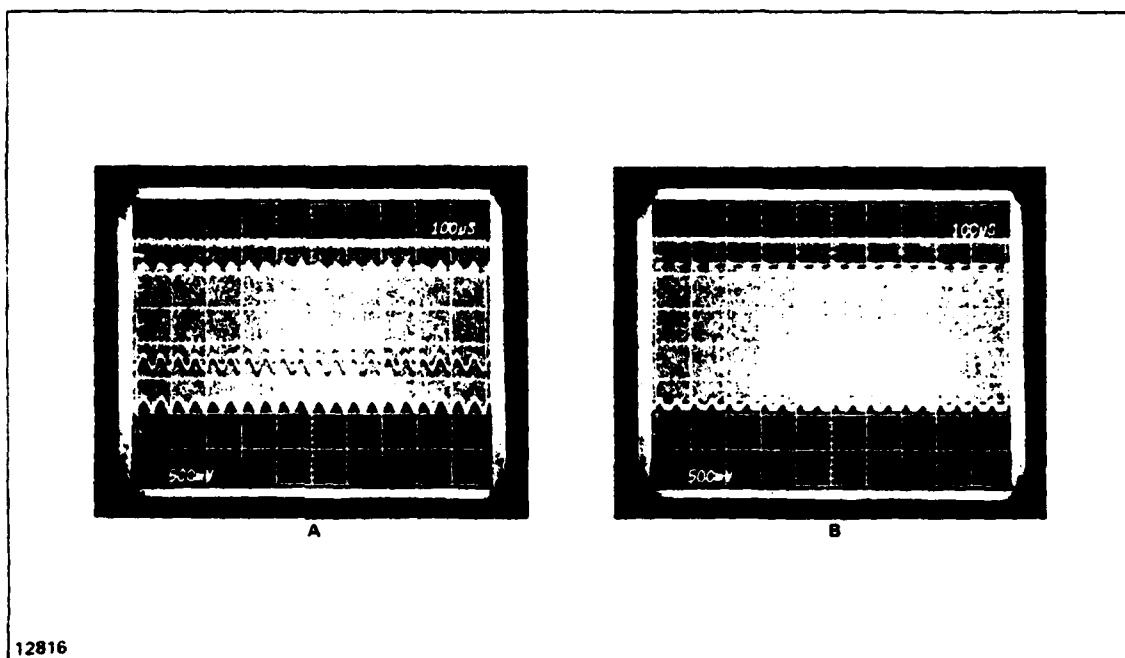


Figure 5-8 - Output Signals with Equilibration Times of 110 ns A) and 5 ns B) for a CCD with Medium Length Input Gates

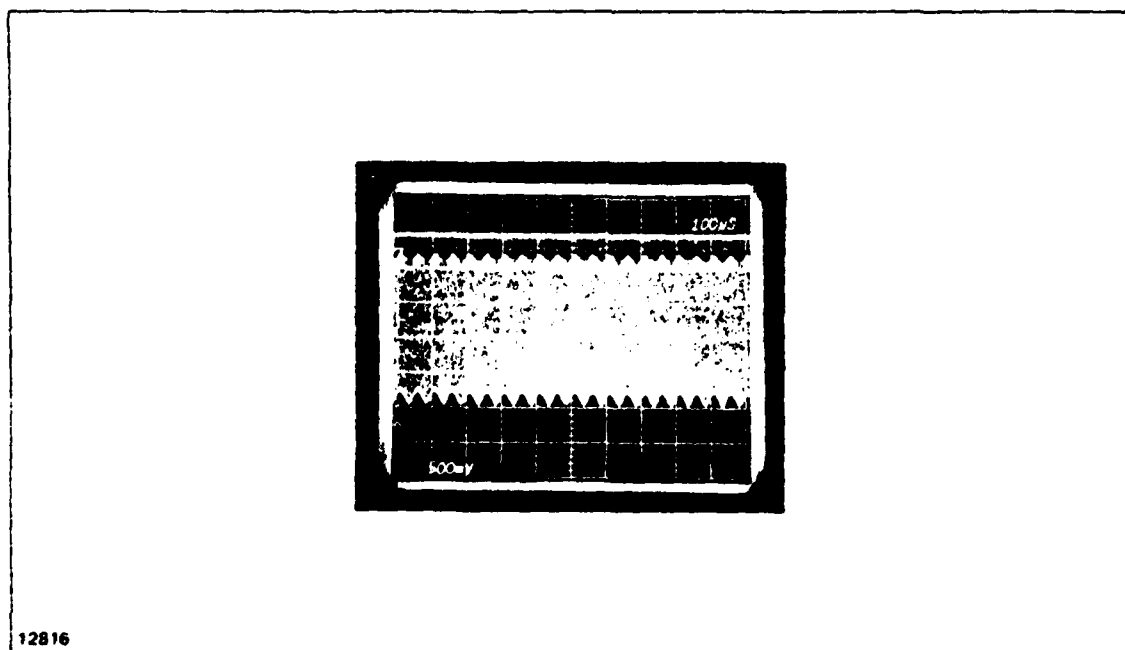


Figure 5-9 - Output of Figure 5-9B After Adjusting the DC Level of the Input Signal

Figure 5-8A and 5-9 are shown in Figure 5-10; they are virtually identical. The most extreme example is shown in Figure 5-11, where the fill time was 2 ns and the equilibration time about 2 1/2 ns. The input signal bias had to be reduced by 0.7 V compared to the value for long fill and spill times. Thus a device with input gates 8.5 μ m and 11.5 μ m long could operate using a potential equilibration input at a frequency above 100 MHz. Of course, full equilibration is not occurring, and some of the advantages of the potential equilibration method will be lost.

In order to get a quantitative measure of the speed of equilibration, we measured the amount of input signal bias shift required to preserve the fidelity of the output signal as the equilibration time was varied. Plotting the results on semi-log paper gave remarkable curves, as shown in Figure 5-12. We were even more surprised when we replotted the theoretical results of Chapter 2 on semi-log paper and found the same behavior.

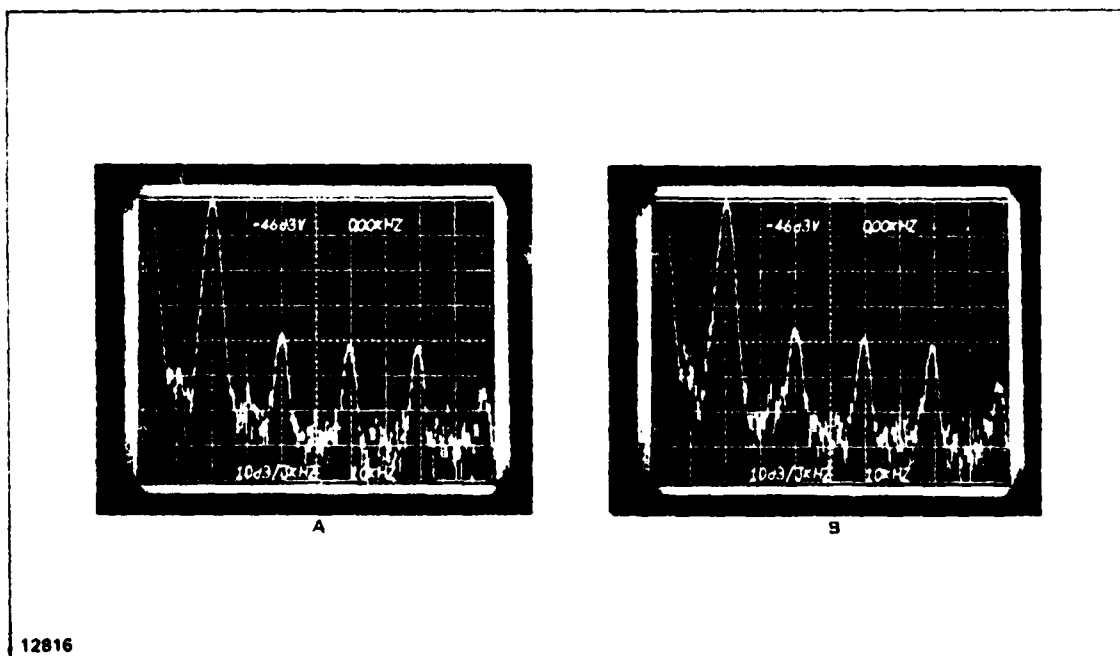
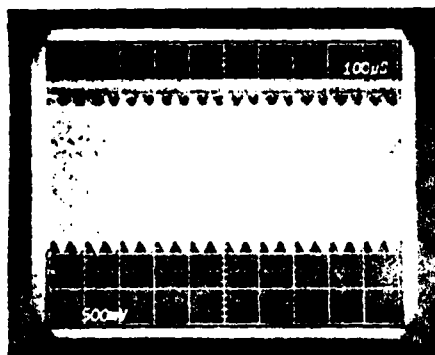
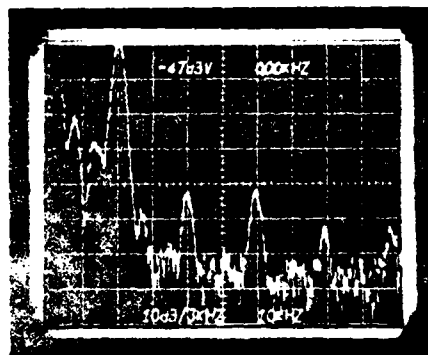


Figure 5-10 - Spectra Corresponding to Figure 5-9B (left) and 5-10 (right)



A



B

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Figure 5-11 - Output Signal A) and Spectrum B) for a Medium Gate CCD with a 2 ns Long Sample Pulse and 2 1/2 ns of Equilibration Time

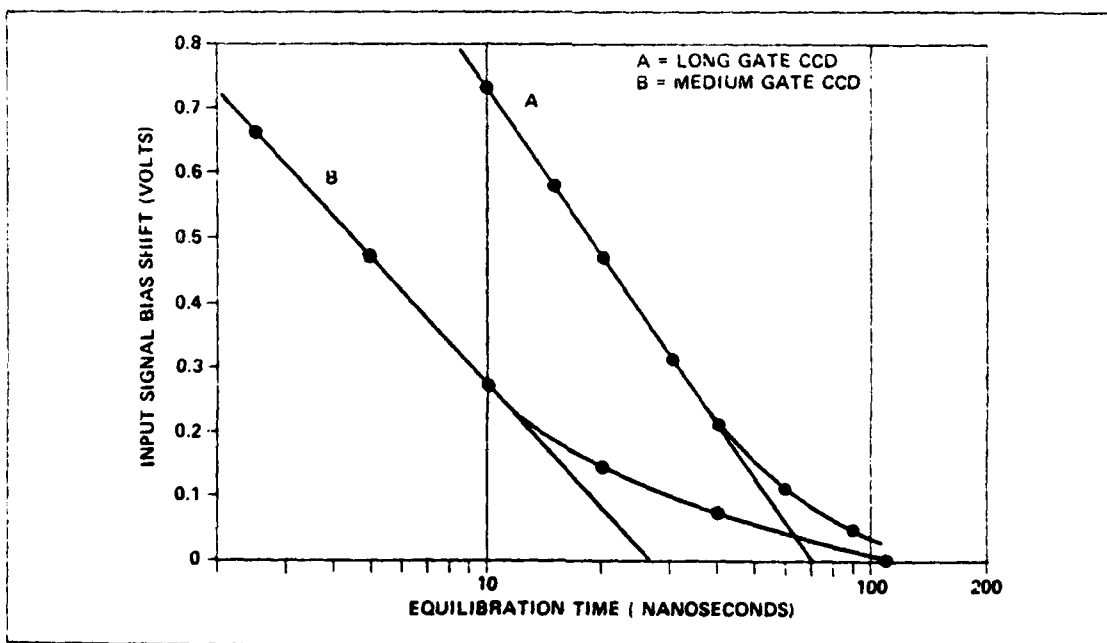


Figure 5-12 - Dependence of Input Signal Bias Offset on Equilibration Time

It is reasonable to suppose that the slope of the curve depends on the amount of overfilling during the fill phase of the input cycle. This accounts for the difference in slopes of the two curves in Figure 5-12, since the conditions for the two CCD's were probably not the same. The intercept with the time axis, however, should be a good relative measure of the equilibration time for the structures. The theoretical results of chapter 2 indicated that the equilibration time should be proportioned to the length of the reference gate (IG_1) and to the input well gate (IG_2). The values of these lengths for Figure 5-13 were $1\text{ }\mu\text{m}$ and $5\text{ }\mu\text{m}$ respectively. Applying the appropriate factors to the 1.6 ns intercept using the gate lengths from Table 5-1 gives intercepts of 31 ns and 71 ns for the medium and long gate CCD's respectively, very close to the experimental values of 26 ns and 69 ns .

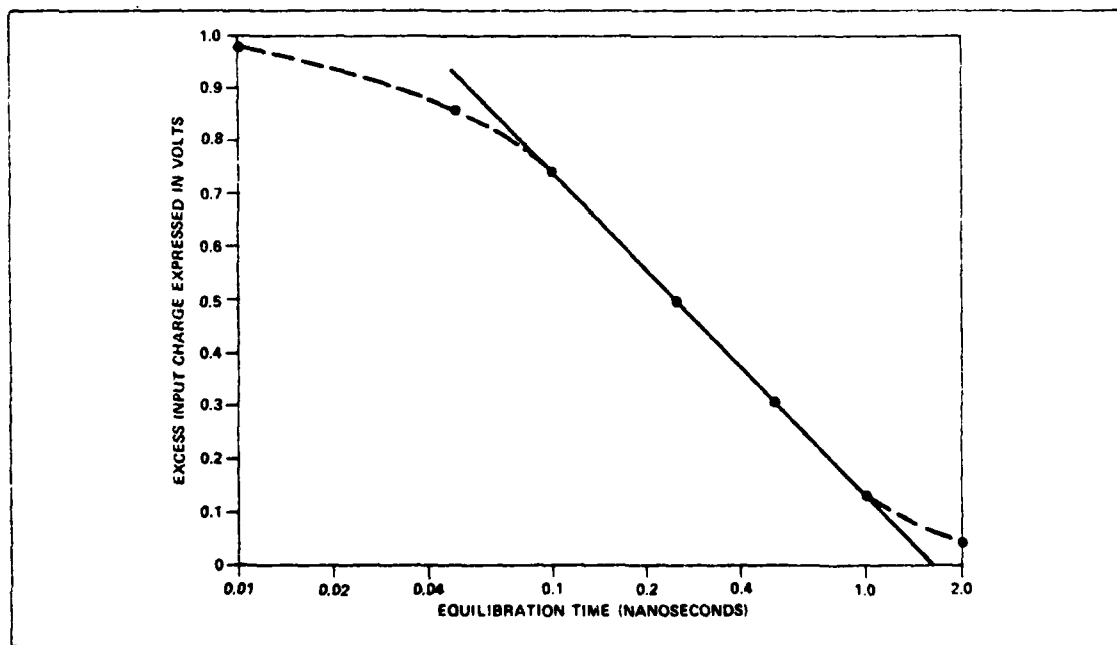


Figure 5-13 - Excess Input Charge Expressed in Volts

5.2.4 Conclusions

Although the amount of data obtained was limited by poor device yield resulting from processing problems, the data, not only was in qualitative agreement with the theoretical results of Chapter 2, but also agreed to a remarkably quantitative degree. There is little doubt that the ECMOS input/output devices, had they been fabricated successfully, would have been capable of operation at frequencies well above 100 MHz.



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